Freedom-to-Operate Intro Scan

Cu-Cu Hybrid Bonding Chip Stacking Process

Case PATTI-FTO-SAMPLE-HYB · 2026-07-31 · Patti by Empryon

AI-ASSISTED TECHNICAL ASSESSMENT — NOT A LEGAL OPINION

SAMPLE REPORT — format illustration on a generic example technology. Not a client engagement.

IMPORTANT NOTICE

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The screening is sample-based: only the patents listed in the Search Log and Patents Reviewed sections were examined. Absence of a reference in this report does not mean no relevant patent exists.

Patent numbers, titles, assignees, dates and claims text are retrieved from public sources and each entry carries a link for independent verification. Relevance assessments and observations are AI-generated reasoning and may be wrong.

Consult a registered patent attorney before making any filing, launch, or freedom-to-operate decision.

1. Subject & Standardized Technical Features

Subject under screening (as confirmed by the requester):

A wafer-to-wafer and die-to-wafer chip stacking process for advanced semiconductor packaging using copper-to-copper hybrid bonding (direct bond interconnect). Dielectric surfaces are planarized by chemical-mechanical polishing and activated by plasma treatment, the surfaces are bonded at room temperature, and a post-bond anneal causes embedded copper pads on both sides to expand and form direct metallic interconnects without solder microbumps. The process includes sub-micron alignment and anneal profile control. Primary patent exposure of interest: United States patents.

Stated target market jurisdiction(s): US — deep-review slots are prioritized for patents enforceable there (WO/PCT next); out-of-jurisdiction documents reviewed after. Family members in the target jurisdiction are not resolved by this tier — check via each patent's link.

Feature	Name	Description (claim-comparable)
TF1	Copper-to-copper hybrid bonding interconnect	Embedded copper pads on two substrates form direct metallic interconnects without solder microbumps, using copper-to-copper direct bond interconnect (DBI) technology
TF2	Dielectric surface planarization	Chemical-mechanical polishing (CMP) planarizes dielectric surfaces prior to bonding to achieve required surface flatness
TF3	Plasma surface activation	Dielectric bonding surfaces are activated via plasma treatment to enable room-temperature bonding
TF4	Room-temperature bonding step	Wafer-to-wafer or die-to-wafer surfaces are joined at room temperature prior to thermal processing
TF5	Post-bond anneal for copper expansion	A controlled post-bond anneal profile causes embedded copper pads on both bonded surfaces to expand and fuse into continuous metallic interconnects
TF6	Sub-micron alignment control	Alignment system achieves sub-micron precision registration between die/wafer pairs prior to bonding

2. Methodology & Screening Funnel (auditable)

Real patent-database search via Google Patents index. Funnel: 226 unique hits searched → 226 relevance-screened (every hit) → 129 flagged as potentially relevant → 40 claims-reviewed in depth (every one with actual claims text) · 1 flagged hits had unretrievable claims and did not consume review slots (listed below). 97 screened out as low-relevance/irrelevant. Every patent cited below originates from these searches — none are AI-generated.

Query	Hits	Source
copper-to-copper hybrid bonding wafer-to-wafer direct bond interconnect	40	searchapi
die-to-wafer hybrid bonding dielectric CMP plasma activation anneal	40	searchapi
room temperature copper hybrid bonding post-bond anneal expansion interconnect	40	searchapi
hybrid bonding sub-micron alignment copper pad expansion	40	searchapi

semiconductor packaging		
direct bond interconnect without solder microbumps copper pad anneal	40	searchapi
wafer bonding plasma activated dielectric surface copper interconnect fusion	40	searchapi

Flagged and prioritized, but claims text could not be retrieved automatically — these did NOT consume deep-review slots (replacements were pulled from the flagged list); review manually via the links:

Patent	Title	Screen relevance
US8183127B2	Method for bonding wafers to produce stacked integrated circuits	MEDIUM

Flagged but not deep-reviewed (over the disclosed review cap of this tier) — listed for transparency; consider a higher tier or manual review:

Patent	Title	Screen relevance
US20240145459A1	Three dimensional integrated circuit with interconnect network layer	MEDIUM
US11721663B2	Multi-level stacking of wafers and chips	MEDIUM
US20250006689A1	Structures and methods for bonding dies	MEDIUM
US20250112123A1	Through substrate via structures and processes	MEDIUM
US12125959B2	Bonding interface for hybrid TFT-based micro display projector	MEDIUM
US20230170327A1	Integrated packaging architecture with solder and non-solder interconnects	MEDIUM
US20140145328A1	Interconnect assemblies and methods of making and using same	MEDIUM
US20080305624A1	Bonding Structure With Buffer Layer And Method Of Forming The Same	MEDIUM
US20100052174A1	Copper pad for copper wire bonding	MEDIUM
WO2020140212A1	Plasma activation treatment for wafer bonding	HIGH
WO2025006069A1	Conductive materials for direct bonding	HIGH
TW202427749A	Directly bonded metal structures having aluminum features and methods of ...	HIGH
CN117855189A	Multilayer substrate based on metal-inorganic medium hybrid bonding and ...	HIGH
JP2025542482A	Direct bonded metal structure with aluminum features and method of making same	HIGH
KR101201087B1	3d integration structure and method using bonded metal planes	HIGH
TW202406082A	High-performance hybrid bonded interconnect	HIGH

	systems	
CN102169845B	A multi-layer hybrid synchronous bonding structure and method for three- ...	HIGH
CN119318220A	Multi-die-to-wafer hybrid bonding	HIGH
KR102531322B1	Integrated circuit package and method	HIGH
TWI702659B	Conductive barrier direct hybrid bonding	HIGH
CN104037102A	Hybrid Bonding and Apparatus for Performing the Same	HIGH
CN110970407B	Integrated circuit package and method	HIGH
JP2026502059A	Structures and processes for void-free hybrid bonding	HIGH
CN112956011B	Layer structure for direct intermetallic bonding at low temperatures in ...	HIGH
TWI870352B	Methods of forming a microelectronic assembly and microelectronic assemblies	HIGH
CN121816110A	Molded direct bond and interconnect stack	HIGH
EP4736224A1	Methods and structures for low temperature hybrid bonding	HIGH
TWI834682B	Molded direct bonded and interconnected stack	HIGH
CN104867895B	Wafer joint technology and structure	HIGH
CN115527992A	Wafer stacking and three-dimensional integrated device structure and method of ...	HIGH
TW202445815A	Semiconductor element with bonding layer having low-k dielectric material	HIGH
CN121464757A	Conductive material for direct bonding	HIGH
KR20260032934A	Method and structure for low-temperature hybrid bonding	HIGH
EP4449492A1	Structure with conductive feature for direct bonding and method of forming same	HIGH
TW202238765A	Contact structures for direct bonding	HIGH
KR20210008917A	Large metal pad on the TV	HIGH
TWI867594B	Dbi to si bonding for simplified handle wafer	HIGH
EP3945566A1	A method for wafer to wafer hybrid bonding, enabling improved metal-to-metal ...	HIGH
TW202429526A	Rapid thermal processing for direct bonding	HIGH
TW202510260A	Structures and methods for bonding dies	HIGH
TW202201583A	Method of fabricating package structure	HIGH

KR20250044724A	High-performance hybrid bonding interconnect system	HIGH
TW202027136A	Plasma activation treatment for wafer bonding	HIGH
CN109830490B	Hybrid junction structure and method for manufacturing the same	HIGH
TW202501764A	Semiconductor element with bonding layer having functional and non-functional ...	HIGH
TWI835746B	Chemical mechanical polishing for hybrid bonding	HIGH
TWI898184B	Semiconductor package and method of forming the same	HIGH
TW202109811A	Semiconductor structure and manufacturing method thereof	MEDIUM
JP5957030B2	Multi-chip package and method for providing multi-chip package die-to-die ...	MEDIUM
CN104752366A	Structure and method of manufacturing 3D integration scheme	MEDIUM
CN116190358A	Stacked semiconductor device and manufacturing method thereof	MEDIUM
JP2023022078A	Bonded structures with integrated passive component	MEDIUM
EP4468345A2	Large metal pads over tsv	MEDIUM
TW202310166A	Bond pads for semiconductor die assemblies and associated methods and systems	MEDIUM
CN220895506U	Semiconductor package	MEDIUM
TWI727523B	Package structure and method of manufacturing the same	MEDIUM
TWI565014B	Semiconductor device and method of manufacturing same	MEDIUM
TWI856375B	Method of forming a microelectronic assembly	MEDIUM
JP7121137B2	Multi-chip package with offset 3D structure	MEDIUM
TW202329389A	Selectable monolithic or external scalable die-to-die interconnection system ...	MEDIUM
CN115707258B	Bond pads for semiconductor die assemblies and associated methods and systems	MEDIUM
TW202406069A	Method for implementing high-precision heterogeneous integration chip	MEDIUM
TWI803310B	Integrated circuit device and methods of forming the same	MEDIUM
EP4666322A1	Interposer for backside power delivery network	MEDIUM

TW202341399A	Integrated circuit package and method of forming same	MEDIUM
KR20240048730A	Semiconductor package	MEDIUM
TW202347662A	Integrated circuit packages and methods of forming the same	MEDIUM
CN112420659B	Semiconductor structure and method for manufacturing the same	MEDIUM
CN112530912A	Package with a metal layer	MEDIUM
CN104752337B	Semiconductor structure and forming method thereof	MEDIUM
TWI814027B	Semiconductor package and method of manufacturing semiconductor package	MEDIUM
TW202401728A	Semiconductor structure and methods for forming the same	MEDIUM
TWI670778B	Package structures and methods of forming the same	MEDIUM
TW202510240A	Multichannel memory with serdes	MEDIUM
TWI783269B	Package, semiconductor package and method of forming the same	MEDIUM
EP4510176A1	Method for assembling eic to pic to build an optical engine	MEDIUM
JP6177766B2	Semiconductor wafer bonding incorporating electrical and optical interconnects	MEDIUM
KR20230119736A	Image sensor device	MEDIUM
TW202516640A	Semiconductor device with interconnects formed through atomic layer deposition	MEDIUM
CN117594569A	Quasi-monolithic die architecture	MEDIUM
TWI830470B	Semiconductor device assemblies including monolithic silicon structures for ...	MEDIUM
TW202331983A	Diffusion barriers and method of forming same	MEDIUM
CN113410133B	Technology used to process the device	MEDIUM
CN122002817A	High-bandwidth memory stack with side interconnects and a three-dimensional ...	MEDIUM
CN113782520A	Die stack structure and method of making the same	MEDIUM
CN110875192A	Wafer level packaging method and packaging structure	MEDIUM
JP2024545355A	Directly bonded frame wafer	MEDIUM
TW202221885A	Package device having extended seal ring	MEDIUM

	structure and method of forming the ...	

This is a screening funnel, not an exhaustive legal clearance search.

3. Patents Reviewed (claims-level)

> ⚠ **AI REASONING — MAY BE WRONG.** The relevance grades, overlap points and distinguishing points below are AI analysis of the actual claims text. Verify each patent via its link before relying on any statement.

3.1 US12532780B2 — Hybrid bonding for semiconductor device assemblies

Assignee: Micron Technology Inc · Published: 2026-01-20 · Status: Active · exp. 2044-04-13 · Relevance: HIGH · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1's core structure (first/second semiconductor die each with dielectric region and bond pad, joined via a hybrid bonding interface with a gap-free metal-metal bonding region and gap-free dielectric-dielectric bonding region) broadly reads on the invention's copper-to-copper hybrid bonding interconnect with embedded copper pads and planarized dielectric surfaces bonded between two substrates.
- Claim 2's recitation that bond pads 'comprise copper' overlaps with the invention's copper-to-copper DBI interconnects.
- Claim 3's 'diffusion metal bond' in the metal-metal bonding region potentially overlaps with the invention's post-bond anneal step causing copper pads to expand and fuse into continuous metallic interconnects.
- Claim 5's method steps (providing two dies with dielectric region/bond pad, compressively bonding by facing and aligning first bond pad to second bond pad, then annealing to form the hybrid bonding interface with gap-free metal-metal and dielectric-dielectric regions) broadly overlap with the invention's sequence of alignment, room-temperature bonding, and post-bond anneal for copper fusion.
- Claim 5's 'aligning the first bond pad to the second bond pad' is a generic alignment limitation that may encompass the invention's sub-micron alignment control as one way of satisfying this broader requirement.
- Claim 6's dished profile 'formed in a surface planarization process' for bond pads potentially overlaps with the invention's CMP-based dielectric/pad surface planarization prior to bonding.
- Claim 9's bond pads comprising copper and claim 12's two-stage anneal (dielectric covalent bond formation, then diffusion metal bond formation) potentially overlap with the invention's copper-to-copper fusion achieved via a controlled post-bond anneal profile.
- Claim 13's compressive bonding pressure and claim 14's anneal temperature/duration windows are process parameters that could generically encompass the invention's room-temperature bonding followed by post-bond anneal, depending on actual invention parameters (not specified in the invention description).
- Claim 16 (parallel independent method claim with nitrogen plasma treatment on both bond pads) similarly overlaps broadly with the invention's die-to-wafer/wafer-to-wafer bonding and anneal-driven copper fusion sequence.

Appears to differ (AI reasoning):

- Claims 1, 5, and 16 all require a 'nitrogen gradient' in the dielectric-dielectric bonding region with concentration increasing toward the metal-metal bonding region — the invention description does not mention any nitrogen-based plasma activation chemistry or resulting nitrogen gradient; it only describes generic 'plasma surface activation' for room-temperature bonding, which may or may not involve nitrogen species.

- Claims 5, 9-11, 15, and 16-20 specifically require forming a 'nitrogen rich region' (e.g., copper nitride) in the bond pad(s) via nitrogen plasma exposure, and require this copper nitride to decompose during anneal and diffuse nitrogen into the dielectric region — the invention's plasma activation is described as directed at dielectric bonding surfaces (not bond pads) and does not reference nitrogen plasma or copper nitride formation, so this specific chemical mechanism appears absent from the invention as described.
- Claim 10 requires the copper nitride be formed 'by microwaving the nitrogen plasma' — no such microwave-generated nitrogen plasma step is described in the invention.
- Claim 4's 'dielectric covalent bond' and claim 12's specific two-stage annealing (separately forming covalent dielectric bond then diffusion metal bond) impose a more granular anneal-stage structure not clearly present in the invention's single 'controlled post-bond anneal profile' description.

Note: This is an informational screening comparison only, not a legal or infringement opinion. The patent's independent claims (1, 5, 16) are structurally very close to the invention's copper-to-copper hybrid bonding concept (embedded copper pads, dielectric bonding, alignment, anneal-driven fusion), representing significant potential overlap in the broad architecture. However, nearly all claims are tied to a specific nitrogen-gradient/nitrogen-plasma/copper-nitride chemistry for achieving the bond, which is not mentioned in the invention's feature list. Whether the invention's 'plasma surface activation' step involves nitrogen species is unclear from the description provided and would need clarification, as this is the central limitation distinguishing dependent and even independent claims. A full claims chart against the actual invention implementation (including plasma gas chemistry) would be needed for a more definitive assessment.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The note's distinguishing point about claim 1's nitrogen gradient acknowledges uncertainty ('may or may not involve nitrogen species') but still uses this as the central distinguishing feature for claim 1 and 16, which are independent claims — since claim 1 explicitly requires the nitrogen gradient as a limiting element (narrowing, not broadening), this is actually correctly reasoned as a distinguishing feature (narrower claim, less overlap), so this is not a wrong-direction error, but the note's hedging ('the invention description does not mention... which may or may not involve nitrogen species') introduces speculation beyond the provided invention features, which only state 'plasma surface activation' with no chemistry specified — treating this ambiguity as if it might resolve in favor of overlap is a slight overstatement not fully grounded in evidence.
- The statement that claim 13's compression pressure and claim 14's anneat temperature/duration windows 'could generically encompass the invention's room-temperature bonding followed by post-bond anneal, depending on actual invention parameters (not specified in the invention description)' is speculative since the invention features provide no anneal temperature or pressure data, making this overlap claim unsupported by the evidence rather than merely uncertain.
- The claim that claim 6's 'dished profile formed in a surface planarization process' overlaps with the invention's CMP-based planarization slightly overstates the match, since the invention describes CMP planarizing dielectric surfaces, whereas claim 6 specifically describes a dished profile in the bond pad (metal) itself, a distinct feature not clearly analogous to the invention's dielectric-focused CMP step.

3.2 US10607937B2 — Increased contact alignment tolerance for direct bonding

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2020-03-31 · Status: Active · exp. 2036-12-15 · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1 requires 'directly bonding the first bonding region with the second bonding region' (non-metallic/dielectric surfaces) prior to conductive contact bonding — broadly overlaps with the invention's dielectric surface bonding step (CMP-planarized, plasma-activated dielectric bonding).
- Claim 2 recites bonding the non-metallic regions 'at room temperature,' which overlaps with the invention's room-temperature bonding step.
- Claim 3 recites 'leaving an initial gap... and heating the first and second elements to cause the first elongate contact feature to directly contact the second... contact feature,' which broadly overlaps

with the invention's post-bond anneal causing embedded copper pads to expand and fuse into continuous metallic interconnects.

- Claim 22 recites contact features 'configured to be directly bonded... without application of external pressure,' consistent with the invention's DBI-style bonding without solder microbumps.
- Claim 31 broadly recites contact structures comprising 'a metal,' which would encompass the invention's copper contact structures.
- General direct-bonding framework (non-metallic dielectric bonding regions + conductive contact structures joined via bonding/anneal) overlaps at a high level with the invention's copper-to-copper hybrid bonding architecture.

Appears to differ (AI reasoning):

- Independent claims 1, 5, 9, and 18 all require that the first and second conductive contact features be 'elongate,' oriented 'non-parallel,' and make contact 'at an intersection' between crossing line-type features (or a grid of lines, per claim 25) — a specific geometric configuration for tolerance improvement. The invention's copper-to-copper hybrid bonding uses embedded, precisely registered copper pads aligned via sub-micron alignment control, not intentionally non-parallel/crossing elongate line contacts; this specific intersection-based contact geometry does not appear to be a feature of the invention as described.
- Several claims (6, 11, 12, 18-20, 29-30) impose specific dimensional ranges (width/length ratios, micron ranges) tied to the elongate/crossing-line geometry, which presumes the non-parallel line structure not described in the invention.
- Claims 26-28 require a specific 'central region with outwardly extending conductive segments' and boundary pattern (polygonal/rounded) — a structural limitation not indicated in the invention's pad-based description.
- Claim 32-33 require a TSV positioned beneath the intersection and connecting traces — an added structural limitation not described in the invention's summary.

Note: This patent's core direct-bonding concepts (dielectric-to-dielectric bonding, room-temperature bonding, and heat-induced expansion/contact of conductive features) broadly track hybrid-bonding technology similar to the invention's copper-to-copper DBI approach, which is why several claim limitations show potential overlap. However, every independent claim (1, 5, 9, 18) hinges on a specific 'non-parallel elongate contact feature intersection' geometry designed to increase alignment tolerance — this is a required claim limitation distinct from the invention's precise sub-micron pad-to-pad alignment approach, which appears to align matching copper pads directly rather than relying on intentionally crossed/non-parallel line contacts. This is an informational screening note only, not a legal or infringement/FTO opinion; a full claim chart and attorney review against the complete claim scope (including dependent claims) is recommended.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap section treats claims 1, 2, 3, 22, and 31 as if they present distinct overlaps, but these are all dependent on or part of independent claim 1's core requirement of non-parallel elongate contact features intersecting — a limitation the note's own distinguishing section says is absent from the invention. Citing these sub-elements as 'overlap' while later using the same claim's core limitation to distinguish is internally inconsistent, though not strictly fabrication since each cited clause is textually accurate.
- The distinguishing arguments correctly identify that the invention lacks the specific non-parallel/intersecting elongate contact feature geometry, which is a legitimate distinguishing feature since it is a limitation actually present in the independent claims (narrowing, not broadening) — this is correct-direction reasoning (narrower claim due to added structural limitation), not wrong-direction reasoning, so no FTO logic error here.
- The claim 31 reference is accurate (dependent on claim 18, which requires the intersection geometry), so calling it 'broadly recites contact structures comprising a metal' without immediately noting its dependency on the non-parallel intersection limitation is slightly overstated/imprecise, since claim 31 cannot be read in isolation from claim 18's core geometry requirement.

3.3 US20250079364A1 — Methods and structures employing metal oxide for direct metal bonding

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2025-03-06 · Status: Pending · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 2 recites direct bonding of dielectric surfaces at room temperature, which corresponds broadly to the invention's room-temperature bonding step prior to thermal processing.
- Claim 3 recites annealing the bonded elements to directly bond the first and second conductive features together, which broadly reads on the invention's post-bond anneal causing embedded copper pads to expand and fuse into continuous metallic interconnects.
- Claim 4 specifies the conductive metal as copper with anneal temperature below ~250°C, which is a generic/broad limitation potentially encompassing the invention's controlled post-bond anneal profile for copper.
- Claims 19-20 describe a bonded structure where first and second conductive features (including copper) are directly bonded to form a bonded contact — broadly consistent with the invention's copper-to-copper DBI interconnect concept, subject to the metal oxide limitation noted below.

Appears to differ (AI reasoning):

- Independent claims 1, 9, and 19 all require a 'metal oxide layer' formed over the first conductive feature and exposed at (or disposed at) the bonding surface, acting as an intermediary bonding-enabling layer between the two conductive features. The invention as described relies on plasma activation of the dielectric surface (not an intentional metal oxide layer on the copper pad) to enable bonding, and does not mention forming, disposing, or exposing a metal oxide layer over the copper pads — this appears to be a required element the invention lacks.
- Claim 19 further requires the bonded contact to have an oxygen content greater than 100 ppm of oxygen in metal within about 100 nm of the bond interface, tied directly to the metal oxide layer's presence — the invention's description does not indicate any deliberate oxygen/metal-oxide content at the interconnect interface.
- Claims 15-18 further narrow the metal oxide layer to nanograin morphology and specific oxidation methods (plasma oxidizing, thermal oxidizing, ozone, wet peroxide) applied to the conductive feature itself — the invention's plasma treatment is described as activating the dielectric surface, not oxidizing the copper conductive feature, suggesting a differing mechanism.

Note: This patent's independent claims are built around an intentionally formed micro-structured/nanograin metal oxide layer over the conductive feature that mediates low-temperature direct bonding and leaves a detectable oxygen signature at the bonded interface. The invention's described process (CMP planarization, plasma activation of the dielectric, room-temperature joining, sub-micron alignment, and post-bond anneal for copper-to-copper fusion) overlaps generically with the room-temperature bonding and anneal-to-fuse-conductive-features limitations (claims 2, 3, 19-20), but the claims' core enabling feature — a metal oxide layer over the conductive feature — is a required element not clearly present in the invention as described, which is a plasma-dielectric-activation-based direct Cu-Cu DBI approach. This is an informational screening note only, not a legal or infringement opinion; verification of whether the invention's plasma treatment or copper surfaces incidentally produce a qualifying metal oxide layer would require further technical review. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The note's overlap section correctly ties claims 2, 3, 4, and 19-20 to the invention's room-temperature bonding, anneal-to-fuse, and copper-to-copper concepts, which is reasonably supported.
- The distinguishing point that the invention lacks a 'metal oxide layer' element required by claims 1, 9, and 19 is factually supported by the evidence (invention describes plasma activation of dielectric, not metal oxide formation on the conductive feature), but the note frames this as reducing FTO risk. This is a wrong-direction inference: pointing out an additional required element in the patent's claims that the

invention doesn't have is a valid non-infringement argument (narrower claim, invention doesn't meet all elements), so this particular reasoning direction is actually correct for claims 1/9/19 — noting it as 'distinguishing' is appropriate here since it's an element the invention lacks, meaning the invention would NOT infringe these narrower claims. This is correctly reasoned, not a flaw.

- The note appropriately caveats with 'further technical review' language and does not overstate certainty, which is faithful practice.
- The claim 4 anneal temperature limitation (<250°C) is described as 'generic/broad' but is actually a specific numerical limit — calling it generic is a mild overstatement, though not fabrication.
- Overall the note stays within the bounds of the provided claim text and invention features without inventing new limitations or mischaracterizing claim scope in the wrong FTO direction.

3.4 US20240079376A1 — Rapid thermal processing for direct bonding

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2024-03-07 · Status: Pending · Relevance: HIGH · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1's core method — direct bonding of non-conductive field regions without adhesive followed by annealing of conductive features — broadly reads on the invention's copper-to-copper hybrid bonding sequence (dielectric bond then post-bond anneal).
- Claims 2-3's 'gap' between conductive features bridged by expansion during anneal overlaps with the invention's post-bond anneal step causing embedded copper pads to expand and fuse into continuous interconnects.
- Claim 6's 'rapid growth structure connecting the first conductive feature to the second conductive feature in multiple locations' and claim 23's bonded structure with a 'rapid growth structure' at the bond interface potentially overlap with the invention's fused copper interconnects formed via anneal, subject to whether the invention's anneal profile qualifies as 'rapid thermal process' (equivalents caution).
- Claim 23's bonded structure (dielectric-to-dielectric direct bond, copper-to-copper direct bond without adhesive) broadly overlaps with the invention's copper-to-copper DBI structure.
- Claim 26 (first/second elements being wafer or die) generically covers the invention's wafer-to-wafer or die-to-wafer bonding.
- Dependent claims 4, 5, 16, 17 reciting a convection/conduction anneal phase in addition to rapid thermal processing could overlap with a controlled multi-stage post-bond anneal profile if the invention's anneal includes such phases.

Appears to differ (AI reasoning):

- Independent claims 1, 14, and 23 require the anneal to be performed specifically 'by way of rapid thermal process' / 'radiant heating' (e.g., claims 7-8 specify radiant heat lamps; claim 19 specifies 0.5s-5min duration at 200-500°C; claim 20 specifies 10-150°C/s ramp rate) — the invention description states only a 'controlled post-bond anneal profile' without indicating use of radiant/RTP heating, so this limitation may not be met if the invention uses conventional furnace/oven annealing.
- Claims 4, 5, 16, 17 require a distinct convection/conduction heating phase in combination with RTP; the invention's disclosed anneal is described as a single controlled profile, and no such dual-phase (RTP + convection/conduction) process is indicated.
- Claim 12 requires use of a load lock and active cooling after anneal — not indicated in the invention's described features.
- Claim 24's specific evidentiary structures (grain extensions, stress gradient, interdiffused metal atom gradient) and claim 28's CTE mismatch (≥5 ppm difference between device portions) are specific structural/material limitations not indicated in the invention description.

- Claim 10's requirement of an optoelectronic single crystal material device portion paired with Si/quartz/fused silica/sapphire/glass is not indicated in the invention, which describes a general copper-to-copper hybrid bonding interconnect without specifying such device materials.

Note: This patent's independent claims are directed to direct (adhesive-free) bonding of non-conductive field regions followed by an anneal of conductive features characterized specifically as a 'rapid thermal process' (RTP)/radiant heating, with resulting 'rapid growth structures' as evidentiary markers. The invention's copper-to-copper hybrid bonding with CMP planarization, plasma activation, room-temperature bonding, and a subsequent 'controlled post-bond anneal' aligns structurally and sequentially with the claimed method/structure at a general level (bond-then-anneal-to-expand-and-fuse copper features), representing potential overlap on core method/structure elements. However, whether the invention's anneal qualifies as an RTP/radiant-heating step (as opposed to conventional furnace annealing) is unclear from the provided description and is the central point on which overlap with the independent claims would turn — this is a factual/technical determination requiring further characterization of the invention's anneal profile (e.g., ramp rate, heating source, duration) against claims 7-8, 19-20. This is an informational screening note only, not a legal or infringement opinion. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap statement regarding claims 4,5,16,17 (convection/conduction anneal phase) is speculative and hedged with 'if the invention's anneal includes such phases,' which is not indicated anywhere in the invention description — this is a weak/unsupported overlap claim rather than fabrication, but it stretches the evidence.
- The distinguishing point citing claims 7-8, 19, and 20 (radiant heat lamps, specific duration/temperature ranges, specific ramp rates) to argue non-overlap is partly wrong-direction reasoning: these are narrow dependent claims, and the independent claims (1, 14, 23) only require 'rapid thermal process' or 'radiant heating' generically, which is the broader and more legally relevant claim scope for FTO purposes; leaning on the narrower dependent-claim limitations to distinguish is not by itself improper, but the note should have emphasized that the broader independent claim limitation (RTP/radiant heating) is the actual point of uncertainty, which it does note separately, creating some redundancy/imprecision in emphasis.
- The claim 12 distinguishing point (load lock, active cooling) is accurately drawn from the claim text, but since claim 12 is dependent and narrow, using it as a general distinguishing point for FTO risk is less significant than addressing independent claim scope; this is a minor imprecision in weighting rather than fabrication.
- The statement that claim 26 'generically covers' wafer-to-wafer or die-to-wafer bonding is faithful to the claim text, but combined with the note's overall structure, the overlap section appropriately identifies broad independent claim language as most concerning, which is correct FTO direction logic overall.

3.5 US20240304593A1 — Direct bonding methods and structures

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2024-09-12 · Status: Pending · Relevance: HIGH · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1 recites a dielectric bonding surface with a conductive feature exposed, planarized to a degree suitable for direct bonding — reads broadly on the invention's CMP planarization step prior to bonding.
- Claim 1 recites exposing the dielectric bonding surface to products of a water vapor plasma prior to direct bonding — overlaps with the invention's plasma surface activation step, though the invention's disclosure is generic 'plasma treatment' while the claim specifies water vapor plasma; this is a potential overlap area with an equivalents-type caution if invention's plasma is water-vapor-based or encompassed by it.
- Claim 3 recites providing a second element with a second dielectric bonding surface and conductive feature, and directly bonding the two dielectric surfaces together — overlaps with the invention's die/wafer-to-wafer copper-to-copper hybrid bonding without solder microbumps.

- Claim 5 recites annealing the bonded elements to form metallic bonds between the first and second conductive features — overlaps with the invention's post-bond anneal step causing embedded copper pads to expand and fuse into continuous metallic interconnects.
- Claim 6 recites positioning the second element such that the first conductive feature is aligned with the second conductive feature prior to bonding — broadly reads on the invention's sub-micron alignment control feature (claim does not specify a precision threshold, so it encompasses sub-micron alignment).
- Claim 7 recites conductive features recessed below the dielectric bonding surfaces on both elements — a hybrid-bonding structural feature that may overlap with the invention's embedded copper pad configuration.
- Claim 8 recites a specific pre-anneal distance (12 nm or less) between conductive features — potential overlap if invention's DBI process achieves comparable pre-anneal spacing, though this is a narrower limitation than the other claims.
- Claim 9/29 recite annealing at temperature less than 200°C — potential overlap with the invention's 'controlled post-bond anneal profile' if that profile falls under 200°C.
- Claim 14 recites the conductive feature comprises copper — directly overlaps with the invention's copper-to-copper hybrid bonding interconnect.
- Claim 15 explicitly recites 'directly hybrid bonding' the first and second elements, encompassing the invention's copper-to-copper hybrid bonding interconnect (DBI) approach.
- Claim 22 recites room temperature bonding of the dielectric surfaces to form an initial bonded structure, followed by annealing to form metallic bonds — closely overlaps with the invention's room-temperature bonding step followed by post-bond anneal for copper expansion/fusion.
- Claim 23–25, 28 recite a generic method of exposing a surface to water vapor plasma products and directly (hybrid) bonding to a second element with subsequent annealing to form metallic bonds — broad claim language that appears to encompass the invention's overall bonding process flow.

Appears to differ (AI reasoning):

- Independent claims 1, 15, and 23 specifically require plasma activation using 'products of a water vapor plasma' (optionally combined with carrier gas or preceded by oxygen plasma per claims 16, 17, 19); if the invention's plasma surface activation uses a different plasma chemistry (e.g., pure oxygen, nitrogen, or argon plasma) rather than water-vapor-based plasma, this specific chemistry requirement may not be met — the invention description does not specify plasma species, so this cannot be confirmed either way.
- Claim 8 requires a specific quantitative pre-anneal gap (12 nm or less) between conductive features — if the invention's DBI process does not achieve or specify this precise dimensional tolerance, this narrow dependent limitation would not be met, though this only affects this specific dependent claim, not the broader independent claims.

Note: This patent's claim set is closely aligned with the invention's overall hybrid bonding process flow (CMP planarization, plasma activation, room-temperature bonding, post-bond anneal for copper-copper metallic fusion, and aligned conductive features). The primary distinguishing feature across the independent claims is the specific requirement of 'water vapor plasma' as the activation chemistry — the invention description only states generic 'plasma surface activation' without specifying the plasma species, so whether this element is met cannot be determined from the provided invention description alone. Sub-micron alignment precision is not explicitly claimed as a threshold but is encompassed by the broader 'aligned' language in claim 6. This is an informational screening note only, not a legal or infringement opinion. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The distinguishing point about claim 8's 12 nm pre-anneal gap is used to suggest non-overlap if the invention doesn't meet this narrow dependent limitation, but this is a dependent claim and irrelevant to whether broader independent claims 1/15/23 are infringed; framing it as a meaningful distinguishing point is somewhat misleading since dependent claims are always narrower and their non-infringement

doesn't reduce risk from independent claims (minor wrong-direction framing, though the note does caveat this).

- The note's distinguishing discussion of water vapor plasma chemistry is appropriately hedged as indeterminate, but then the concluding paragraph states 'The primary distinguishing feature across the independent claims is the specific requirement of water vapor plasma' as if this were an established distinguishing feature, when the note itself admits it cannot be confirmed either way — this is an overstatement/inconsistency, since an unconfirmed limitation should not be characterized as 'the primary distinguishing feature.'
- The statement that claim 6 'does not specify a precision threshold, so it encompasses sub-micron alignment' is reasoning that broader claim language covers the invention's feature, which is correct direction for overlap, but then this same broad-claim logic is inconsistently not applied with equal weight to undercut the water-vapor-plasma distinguishing argument, creating a minor internal inconsistency in how claim breadth is treated across the note.

3.6 US20250096191A1 — Direct bonding methods and structures for dies

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2025-03-20 · Status: Pending · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1 broadly recites 'direct bonding at least one of the plurality of dies to a second substrate' after preparing a surface for direct bonding, which is a generic direct-bonding step that could encompass the invention's copper-to-copper hybrid bonding process depending on how 'direct bonding' is implemented.
- Claim 3 recites direct bonding a first conductive element (in a first dielectric portion) to a second conductive element (in a second dielectric portion) on the second substrate — this broad conductor-to-conductor plus dielectric-to-dielectric direct bonding language could read on the invention's copper pad-to-copper pad and dielectric-to-dielectric hybrid bonding interconnect, especially since no specific bonding temperature, activation method, or anneal is required by this claim.
- The claims' 'preparing a first surface... for direct bonding' step is generic and could encompass surface preparation steps such as CMP planarization and/or plasma activation used in the invention, since no specific preparation technique is excluded.
- Apparatus claim 12 covers a die directly bonded to a substrate via a bonding surface, which could overlap with the invention's bonded die/wafer structure if the invention's die also includes an unpatterned backside dielectric layer forming the second side.

Appears to differ (AI reasoning):

- Independent claims 1 and 23 require thinning the first substrate after surface preparation and depositing/forming a 'stress balancing layer' on the thinned second surface prior to singulation — the invention description does not mention any substrate thinning step or a stress balancing layer, so this specific process sequence appears to be a required limitation the invention lacks.
- Claim 23 further requires determining a bow of the first substrate and calculating/determining a stress-balancing-layer thickness based on that measured bow — the invention's described alignment and bonding process does not include any bow measurement or stress-compensation calculation step.
- Apparatus claims 12–22 require a 'backside dielectric layer' forming the second side of the die (in some claims specifically unpatterned, or with defined thickness/perimeter relationships) — the invention as described does not include such a backside dielectric layer feature.
- Claims 15–16 require multiple dies bonded with a lateral gap and a reconstitution layer filling that gap — no such multi-die reconstitution structure is described in the invention.

Note: This patent's claims center on a specific process of thinning a substrate and depositing/forming a stress-balancing dielectric layer on the thinned backside prior to singulation and direct bonding (claims 1, 23), plus apparatus claims requiring a backside dielectric layer on the bonded die (claims 12-22). The

invention's described features (CMP planarization, plasma activation, room-temperature copper-to-copper bonding, post-bond anneal, sub-micron alignment) are not mirrored by these specific limitations, but claim 3's broad recitation of direct bonding a conductive element to a conductive element and dielectric to dielectric (without specifying activation method, temperature, or anneal) is broad enough to warrant a closer look for potential overlap with hybrid copper bonding implementations. Overall relevance is medium: the patent is in the same direct/hybrid bonding technical space but its core distinguishing claim elements (thinning + stress balancing layer, bow-based thickness determination) are absent from the invention description as given. This is an informational screening only, not a legal or infringement conclusion; full claim charting against complete invention documentation is recommended. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap statements are appropriately hedged and traceable to claims 1, 3, and 12, but the note treats the absence of thinning/stress-balancing-layer limitations (claims 1, 23) as a clean distinguishing point without flagging that claim 3, which depends from claim 1 and thus inherits claim 1's thinning/stress-balancing-layer limitations, would also require those elements for actual infringement risk — the note's discussion of claim 3 as a standalone broad overlap risk somewhat understates that claim 3 is dependent and carries forward claim 1's narrower requirements, which is a minor accuracy/precision issue in the overlap analysis.
- The distinguishing points about claims 1, 23, and 12-22 requiring elements (thinning, stress balancing layer, bow measurement, backside dielectric layer, lateral gap/reconstitution layer) that the invention lacks are reasoning in the correct direction (invention lacks an element required by the claim, so claim doesn't read on invention) and are supported by the claim text, so these are not wrong-direction reasoning errors.
- The note's claim that claim 1's 'direct bonding' step and the 'preparing a first surface... for direct bonding' step are 'generic' and 'could encompass' CMP planarization or plasma activation is a reasonable but speculative inference not explicitly confirmed by the abstract/claims, though it is appropriately hedged with qualifying language.

3.7 US12604771B2 — Direct bonding methods and structures

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2026-04-14 · Status: Active · exp. 2043-10-31 · Relevance: HIGH · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Direct copper-to-copper (contact feature-to-contact feature) bonding without intervening adhesive, as in claims 1, 11, and 18, appears broad enough to encompass the invention's copper-to-copper DBI hybrid bonding of embedded pads.
- Claim 9 recites bonding nonconductive field regions at room temperature followed by an anneal to increase bond strength, which overlaps with the invention's room-temperature bonding step followed by a post-bond anneal that expands/fuses copper pads.
- Claim 17 recites polishing the first bonding surface prior to further processing (protective layer application, singulation), which overlaps generically with the invention's CMP planarization of dielectric surfaces prior to bonding.
- The claims' direct bonding of nonconductive field regions together with contact features (hybrid bonding structure) overlaps conceptually with the invention's combined dielectric/copper hybrid bonding scheme.

Appears to differ (AI reasoning):

- Independent claims 1 and 11, and dependent claims 2, 12, and 16, affirmatively require that the first bonding surface NOT be exposed to a plasma before/after processing and before direct bonding, using liquid etchant/chemical (e.g., HF) and terminating liquid treatments (e.g., TMAH, glass-forming solutions) instead — this appears to conflict with the invention's plasma surface activation step, which the claims seem to expressly exclude as a bonding-surface preparation method.

- The claims require specific chemical surface preparation steps (liquid etching with HF, terminating liquid treatment with TMAH, boron-containing or glass-forming solutions) as activation mechanisms; the invention's description does not indicate use of these particular liquid chemical treatments, relying instead on plasma activation, which the claims do not use as an activation mechanism in the recited method steps.
- Claim 17 requires a protective layer applied after polishing and prior to singulation into dies, with later removal of that protective layer without plasma exposure — the invention's described process does not mention a protective layer/singulation sequence, so this specific claim limitation may not be met, though this affects only claim 17's specific method, not claims 1/11 generally.

Note: This patent's independent claims (1, 11, 17) are directed to direct/hybrid bonding methods using liquid chemical etching and termination treatments, several of which explicitly exclude plasma exposure as part of the claimed method. Because the invention affirmatively employs plasma surface activation to enable room-temperature bonding, there is a notable tension with the plasma-exclusion limitations recited in claims 1, 2, 11, 12, and 16. However, other aspects of the claims — direct bonding of contact features and field regions without adhesive, room-temperature bonding followed by anneal (claim 9), and pre-bond polishing (claim 17) — are broadly worded and could still read on corresponding invention features. This is an informational screening note only; a full claim-by-claim legal analysis, including review of surface-activation equivalents and prosecution history, would be needed for a definitive assessment.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap statement regarding claim 17's 'polishing the first bonding surface prior to further processing' overlapping with the invention's CMP planarization is overstated: claim 17 requires polishing followed specifically by protective layer application and singulation into dies, a sequence not present in the invention features; characterizing this as 'generic' overlap glosses over the specific claim structure.
- The note's overlap claims for claims 1, 11, and 18 do not acknowledge that these claims also require the plasma-exclusion and liquid etch/terminating treatment limitations as integral parts of the same claim (not separable), which the note itself flags as distinguishing later — creating some internal tension in how 'overlap' is framed versus 'distinguishing' for the same claims.
- The distinguishing point about the invention lacking a protective layer/singulation sequence (claim 17) is a correct non-infringement observation for claim 17 specifically, but the note does not address whether this same reasoning undercuts its own claimed 'overlap' with claim 17 for CMP planarization, since claim 17 as a whole would not be met by the invention — this is a minor internal inconsistency rather than fabrication.
- The overall framing correctly identifies plasma-exclusion as a distinguishing feature (correct direction, since narrower claims requiring absence of plasma would not read on a plasma-based invention), so no wrong-direction FTO logic is present; however, the note's concluding paragraph slightly overstates 'tension' as if it were dispositive, when claims 1/11 still contain the plasma-exclusion as a required limitation rather than optional, which actually strengthens the distinguishing argument rather than weakening it as implied by hedging language.

3.8 US11911839B2 — Low temperature hybrid bonding

Assignee: Advanced Micro Devices Inc · Published: 2024-02-27 · Status: Active · exp. 2041-12-28 · Relevance: HIGH · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1/11 recite hybrid bonding between two dies via metallurgical (metal-to-metal) bond pads plus dielectric bonding — this generically encompasses the invention's copper-to-copper DBI interconnect formed on embedded pads within dielectric layers.
- Claim 2/12's 'hybrid bond' combining metallurgical bond pads and a dielectric bond broadly reads on the invention's combination of copper pad bonding and dielectric surface bonding via CMP-planarized/plasma-activated surfaces.
- Claim 5/15 characterizing the metallurgical bond as a 'cold weld' potentially overlaps with the invention's room-temperature bonding step, though the invention additionally applies a post-bond anneal to expand/fuse copper, which is a differing mechanism from a room-temperature-only cold

weld — treated as overlapping under equivalents given both involve low/room-temperature initial metal-to-metal contact.

- Claim 6/16's requirement that bond pad protrusion distances differ prior to bonding (enabling low-temperature/room-temperature bonding) potentially overlaps with the invention's room-temperature bonding step and subsequent anneal-driven expansion, since both approaches aim to reduce required bonding temperature via pad geometry/expansion.
- The apparatus claims' general recitation of dies bonded via bond pads and dielectric layers is broad enough to potentially cover wafer-to-wafer or die-to-wafer configurations described in the invention.

Appears to differ (AI reasoning):

- Claims 1/11 require first bond pads to include a 'base portion and an annular portion plated on the base portion' — a specific pad structure not described in the invention's features, which only mention 'embedded copper pads' without this base/annular plated structure.
- Claims 4/14 require first bond pads to include a 'notch' that mates with protruding second bond pads — a specific geometric mating feature not indicated in the invention's description.
- Claims 6/7/16 require a specific pre-bond distance differential (including a 1-2 nanometer difference in claim 7) between pad protrusion and dielectric surface — the invention's description does not specify such a pad-height differential mechanism, relying instead on CMP planarization and post-bond thermal anneal for expansion.
- Claim 20 requires through-silicon vias coupled to carrier interconnects — not mentioned among the invention's features.
- Claim 3/8/13/17 require specific offset/misalignment relationships between metallurgical bond interfaces and dielectric bond interfaces — no corresponding structural detail is described in the invention.

Note: This patent's claims center on a specific hybrid-bonding pad architecture (base+annular-plated pads within dielectric apertures, protruding mating pads, pre-bond dimensional offsets) that enables cold-weld/low-temperature metallurgical bonding combined with dielectric bonding. The invention's broader description of copper-to-copper DBI with CMP planarization, plasma activation, room-temperature bonding, and post-bond thermal anneal for copper expansion shares the same general hybrid-bonding concept (metallurgical + dielectric bond) and low-temperature bonding goal, creating potential overlap at a conceptual/generic level, particularly around claims 1, 2, 5, 6, 11, 12, 15, and 16. However, several claims impose specific structural limitations (annular plated portions, notches, precise nanometer-scale pad protrusion differentials, TSVs) that are not evidenced in the invention's disclosed features, representing potential distinguishing points if those specific structures are absent. This is an informational screening note only, not a legal or infringement conclusion; a full claim chart and expert comparison of actual pad geometries and process parameters would be needed for further assessment.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap statement for Claim 1/11 elides the required 'base portion and an annular portion plated on the base portion' structural limitation, treating the claim as if it generically covers any embedded copper pads — this overstates overlap since claim 1 is narrower than described in the overlap paragraph (though the distinguishing section later correctly notes this limitation, creating internal inconsistency).
- The distinguishing points for claims 1/4/6/7/20/3/8/13/17 all rely on the claims reciting additional specific structural limitations (annular plated portion, notch, nanometer pad-height differential, TSVs, offset interfaces) NOT present in the invention's features — this is backwards FTO direction logic: a claim with MORE limitations is NARROWER and thus easier to avoid, which actually supports non-infringement correctly here (narrower claim, invention lacks the extra limitation, so no read-on) — this reasoning is actually correctly directed (absence of narrowing feature in invention breaks literal infringement), so it is not wrong-direction; however the note's framing in the overlap section calling claims 1/2 'generic' overlap despite the mandatory annular/base structure is an overstatement not supported by the claim language, which requires that specific structure as an essential element.
- The claim 5/15 'cold weld' overlap discussion introduces an 'equivalents' framing ('treated as overlapping under equivalents') that is not grounded in the provided claim text or invention features — this is speculative characterization beyond the evidence.

3.9 US20240088120A1 — Stacked devices and methods of fabrication

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2024-03-14 · Status: Active · exp. 2039-07-10 · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claims broadly recite 'hybrid bonding' between a sensor element/wafer and a logic element/die, which as a generic term for combined dielectric/metal direct bonding could encompass the invention's copper-to-copper DBI interconnect scheme
- The claims' hybrid bonding layers (e.g., claim 4's 'hybrid bonding layer of the sensor element and an other hybrid bonding layer of the first handle wafer') are broad enough to read on embedded copper pad structures used for direct metallic interconnection as in the invention
- Claim 14's recitation of providing bonding layers on both sides prior to joining could overlap with the invention's dielectric planarization and surface preparation steps prior to bonding, though the claims do not specify CMP or plasma activation explicitly
- General wafer-to-wafer/die-to-wafer bonding steps (claims 1, 13, 15) are broad process steps that could overlap with the invention's room-temperature bonding step as one possible implementation of 'hybrid bonding'

Appears to differ (AI reasoning):

- The claims are directed to a specific overall image-sensor stacking method (bonding sensor to handle wafer, hybrid bonding logic element, removing handle wafer, processing first side with optical features, opening contacts) — the invention as described is a generic bonding interconnect technology without any recited sensor/handle-wafer/optical-feature architecture, so several structural claim elements (optical features, contact opening, handle wafer removal) are not addressed by the invention description
- Claims require specific sequential process steps (e.g., bonding first side to handle wafer, then hybrid bonding logic element, then removing handle wafer, then processing first side) that are not present in the invention's described features, which focus only on the bonding interconnect formation itself

Note: This patent's claims are method claims specific to image-sensor stacked device fabrication (sensor-to-handle-wafer bonding, hybrid bonding to logic dies, optical feature formation, contact opening), whereas the invention description centers on generic Cu-Cu hybrid bonding process technology (CMP planarization, plasma activation, room-temperature bonding, post-bond anneal, sub-micron alignment). The claims' generic term 'hybrid bonding' is broad and could potentially encompass the invention's Cu-Cu DBI process as an underlying bonding technique, representing a possible overlap area requiring equivalents analysis. However, the claims add substantial additional structural/method limitations (sensor/handle wafer arrangement, optical feature deposition, contact opening sequences) that are not described in the invention's feature set, and these appear to be required elements of the claims not obviously present in the invention. This is an informational screening note only, not a legal or infringement conclusion; full claims interpretation and comparison against complete invention documentation would be needed for a definitive assessment.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The note's distinguishing points rely on the invention lacking sensor/handle-wafer/optical-feature elements that the claims recite as required limitations — this is actually correct-direction reasoning (narrower claims with more limitations are easier to design around), so this part is not a logic error. However, the note's overall framing risks conflating 'invention lacks feature X' with 'therefore no overlap,' without acknowledging that the claims' hybrid bonding step could still be infringed if the invention's Cu-Cu DBI method were used within an image-sensor stack meeting all other claim elements; this nuance is stated but somewhat buried.
- The claim excerpt does not explicitly mention 'dielectric surface planarization,' 'plasma activation,' 'room-temperature bonding,' 'post-bond anneal for copper expansion,' or 'sub-micron alignment' at all — the note appropriately flags that these are not explicitly recited, but repeatedly speculates that generic 'hybrid bonding' or 'bonding layers' 'could encompass' or 'could overlap with' these specific process

steps, which is a stretch beyond what the claim text supports; this is an overstatement of overlap likelihood rather than a fabrication, since the note hedges each claim with 'though the claims do not specify' or 'could potentially.'

- The claim of overlap regarding claim 14's 'bonding layers on both sides' being comparable to 'dielectric planarization and surface preparation' is speculative extrapolation not directly supported by the claim language, which only mentions 'providing a first/second bonding layer' without describing planarization or surface prep techniques.

3.10 US12347820B2 — Stacked devices and methods of fabrication

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2025-07-01 · Status: Active · exp. 2039-07-10 · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1 recites 'hybrid bonding' between a connecting wafer/first bonded structure and a logic element, which is a generic term commonly encompassing copper-to-copper direct bond interconnect (DBI) processes as in the invention, representing potential overlap with the invention's hybrid bonding interconnect step
- Claim 2 recites wafer-to-wafer bonding, which broadly reads on the invention's room-temperature wafer-to-wafer or die-to-wafer bonding step
- Claim 12 recites providing a layer of bonding pads as part of electrical connections, which could encompass the invention's embedded copper pads used for direct metallic interconnects
- Claim 3/8/9 contemplate hybrid bonding a logic die (die-to-wafer bonding), overlapping generically with the invention's die-to-wafer bonding scenario

Appears to differ (AI reasoning):

- Claim 1 specifically requires a multi-layer bonded sensor structure with a sensor wafer, connecting wafer, and logic element, plus subsequent processing to add optical features (e.g., filter array, on-chip lens) and opening contacts — the invention as described is a generic copper-to-copper hybrid bonding interconnect process without any recited sensor wafer, optical feature formation, or specific stacked sensor/logic architecture
- The claims require a specific sequence of bonding a connecting wafer to a sensor wafer, then hybrid bonding to a logic element, then processing the sensor wafer's opposite side for optical features — the invention does not describe any sensor-specific or optical-feature-related processing steps
- Dependent claims requiring handle wafer removal (claim 4), thinning of sensor/connecting wafers (claims 5,10), and filter/lens deposition (claims 6,7) impose structural/process limitations tied to image sensor fabrication that are not part of the invention's disclosed generic bonding process

Note: This patent's claims are directed to a specific stacked image-sensor fabrication method using hybrid bonding as one step among several sensor/logic integration steps, whereas the invention describes a generic copper-to-copper hybrid bonding process (CMP planarization, plasma activation, room-temperature bonding, post-bond anneal, sub-micron alignment) without sensor-specific context. The generic 'hybrid bonding' and 'wafer-to-wafer bonding' language in claims 1-2 could broadly encompass the invention's bonding technique, creating potential overlap on that narrow point, but the claims as a whole require additional sensor/logic-specific structure and processing not present in the invention description. Full claim charting against actual invention embodiments and prosecution history would be needed for a definitive assessment.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap/distinguishing analysis is largely faithful to the claim text, but the final summary paragraph's framing ('the claims as a whole require additional sensor/logic-specific structure... not present in the invention description') is used to distinguish the invention from claim 1, which is wrong-direction reasoning: since claim 1 is the broadest independent claim and all limitations (sensor wafer, optical features, contacts) must be met for infringement, the ABSENCE of these elements from the invention actually means the invention likely does NOT infringe claim 1 (correct conclusion), but the note frames

this as the invention lacking features recited in the claim rather than properly noting that a narrower claim with more limitations is easier to avoid — this part is actually correctly reasoned (narrower claim, easier to avoid), so it is not a true direction error, but the note's phrasing conflates 'generic hybrid bonding overlaps' with claim 1's specific narrow scope in a way that risks overstating overlap on claims 1-2, which are anchored to a sensor-wafer-specific method and would not be infringed merely by generic Cu-Cu hybrid bonding outside that context.

- The claim of overlap with claim 12 ('layer of bonding pads... could encompass the invention's embedded copper pads') is speculative and not clearly supported, since claim 12 depends from claim 11/10/1 and is embedded within the specific sensor/connecting-wafer/logic-element structure, not a standalone bonding-pad claim; describing this as overlap without noting the dependency chain limitation is an overstatement.

3.11 US12211820B2 — Wafer bonding apparatus and method

Assignee: Taiwan Semiconductor Manufacturing Co TSMC Ltd · Published: 2025-01-28 · Status: Active · exp. 2042-08-25 · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Independent claims 1, 8, and 14 require a plasma activation process on a wafer surface prior to bonding, which broadly overlaps with the invention's plasma surface activation step for enabling room-temperature bonding of dielectric surfaces
- The claims' 'bonding the first wafer to a second wafer' step is generic wafer bonding language that could encompass the invention's die/wafer bonding step, though the patent does not specify copper pad or hybrid bonding details
- The cleaning process (rinsing with de-ionized water, forming silanol groups) could overlap with pre-bonding dielectric surface preparation steps in the invention, though the invention's CMP planarization is a distinct mechanical step not addressed here

Appears to differ (AI reasoning):

- All independent claims (1, 8, 14) specifically require a plasma grid assembly with distinct coarse mesh and fine mesh regions creating differential (high vs. low) activation regions correlated to crystallographic directions (e.g., <110> vs <100>) — the invention as described does not appear to use a dual-mesh grid or crystallographic-direction-based differential activation scheme
- Claims require formation of silanol groups via a specific cleaning process tied to differential activation regions, which is a chemistry-specific limitation not described in the invention's plasma activation step

Note: This patent's claims are narrowly directed to a specific plasma activation apparatus/method (dual mesh grid producing differential high/low activation regions tied to wafer crystallographic orientation) and associated cleaning chemistry, rather than to copper-to-copper hybrid bonding, CMP planarization, or post-bond copper diffusion/anneal features central to the invention. The generic 'plasma activation' and 'bonding' language in claims 1, 8, and 14 is broad enough to warrant a potential overlap flag for any plasma-activated wafer bonding process, including the invention's room-temperature hybrid bonding, but the specific coarse/fine mesh grid and crystallographic-direction limitations are structural requirements not evidently present in the invention as described. This is an informational screening note only, not a legal or infringement opinion; a full claim-chart analysis with actual process details (e.g., activation tool used) would be needed for a more definitive assessment.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap statement 'broadly overlaps with the invention's plasma surface activation step' is somewhat overstated since all independent claims require the specific coarse/fine mesh differential activation limitation, not merely generic plasma activation — the note does note this later but the initial overlap framing risks overstating breadth before qualifying it.
- The distinguishing point that the claims require the dual-mesh/crystallographic differential activation scheme 'not appear[ing]' in the invention is used to distinguish, but since claims 1, 8, and 14 are narrower (adding this specific limitation) rather than broader, this is correctly reasoned as narrowing rather than wrong-direction; however, the note's overlap section separately claims generic plasma

activation language is broad enough to flag overlap, which is inconsistent with claims actually requiring the narrow mesh/crystallographic limitation in every independent claim — this creates some tension/imprecision about what the claims actually require.

- The statement that 'the patent does not specify copper pad or hybrid bonding details' is used to acknowledge a gap in the patent rather than as a distinguishing feature for invention non-infringement risk; this is accurately framed as reducing overlap likelihood, not as wrong-direction reasoning, so it is acceptable, though listed for completeness.

3.12 US12354911B2 — Cu3Sn via metallization in electrical devices for low-temperature 3D-integration

Assignee: Raytheon Co · Published: 2025-07-08 · Status: Active · exp. 2041-02-25 · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1 requires 'a bonding layer at least partially surrounding the interconnect and at least partially overlying the substrate' made (per claim 3) of a silicon oxide material — this reads on the invention's dielectric bonding surfaces, and claim 16's requirement that an upper surface of the bonding layer be polished to planarize the interconnect with the bonding layer directly overlaps the invention's CMP dielectric planarization step prior to bonding.
- Claim 17-19 describe 3D-integration by bonding two such electrical devices together, with claim 18 reciting bonding layers of the two devices bonded together and claim 19 reciting the electrically conductive interconnects being 'fusion bonded together' — this generic fusion-bonding-of-interconnects concept potentially overlaps with the invention's post-bond anneal causing embedded copper pads to expand and fuse into continuous interconnects, since the claim does not limit the fusion mechanism to a particular composition beyond Cu3Sn but the underlying die-to-die/wafer-to-wafer interconnect fusion concept is analogous.
- Claim 9/10 (via hole as through hole or blind hole) and claim 5 (interconnect directly connected to trace) are broad structural limitations that could read on generic via/interconnect structures similar to those underlying the invention's copper pad interconnects, if such structures are present in an analogous via-based implementation.

Appears to differ (AI reasoning):

- Claim 1 requires the electrically conductive interconnect be 'made of Cu3Sn' formed by 'solid-state diffusion of Cu into Sn' — the invention's interconnects are described as copper-to-copper (Cu-Cu) direct bonds without an intermediate Sn layer or Cu-Sn intermetallic formation, so this core compositional/process limitation appears absent from the invention.
- Claim 12 requires deposition of a Sn layer in the via hole, deposition of Cu atop and in contact with the Sn, and heating below the Sn melting point to cause solid-state diffusion of Cu into Sn — the invention's process (plasma activation, room-temperature bonding, then anneal causing pure copper pad expansion/fusion) does not appear to involve any Sn layer or Cu-Sn diffusion couple.
- Claims 13-15 further narrow the heating step to specific temperature ranges (100-200°C or 100-150°C) tied to Kirkendall void formation in a Cu-Sn system, a mechanism specific to Cu3Sn formation that does not appear present in the invention's pure Cu-Cu anneal process.
- Claim 20 requires the interconnect be Cu3Sn 'without an undesirable phase' such as Cu6Sn5 or Cu4Sn — this phase-control limitation presumes a Cu-Sn intermetallic system entirely absent from the invention's copper-only interconnect.

Note: The patent's claims are centered on a Cu3Sn intermetallic via interconnect formed by Sn/Cu solid-state diffusion, a materially different interconnect chemistry and process from the invention's direct Cu-Cu hybrid bonding (DBI) approach. Structural/process claim elements around bonding layers (dielectric, silicon oxide), CMP planarization of the bonding layer, and 3D-integration via fusion bonding of interconnects show conceptual overlap with the invention's dielectric planarization, plasma activation, and post-bond anneal fusion steps, but the specific composition and formation mechanism (Cu3Sn via Sn-Cu diffusion) required by independent claim 1 and its dependents appears absent from the invention as described. This is an informational screening only, not a legal or FTO conclusion.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap statement on claim 19 concedes that claim 1 requires the interconnect to be Cu3Sn, meaning claim 19's 'fusion bonded together' limitation is dependent on claim 17 which incorporates claim 1's Cu3Sn requirement; characterizing this as 'potentially overlapping' with the invention's pure Cu-Cu fusion is a stretch since the claimed interconnect composition is explicitly Cu3Sn, not generic — this overstates overlap not well supported by the claim text as a whole.
- The overlap statement on claims 9/10/5 speculating these 'could read on generic via/interconnect structures similar to...the invention's copper pad interconnects, if such structures are present in an analogous via-based implementation' is speculative and hedged with a conditional not established by the invention features (which describe pads, not explicitly via holes), bordering on fabricated overlap.
- The claim 16 overlap point is reasonably supported (polishing bonding layer to planarize interconnect) but claim 16 is dependent on claim 1's Cu3Sn interconnect, so framing it as a direct overlap with the invention's CMP step somewhat overstates commonality without acknowledging the compositional context.
- The note's distinguishing points do not rely on absence-of-recitation reasoning in the wrong direction; they correctly note additive limitations (Cu3Sn, Sn diffusion, specific temperature ranges) as narrowing and distinct from the invention's actual described process, which is appropriate direction of reasoning.

3.13 US8524533B2 — Room temperature metal direct bonding

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2013-09-03 · Status: Expired - Fee Related · exp. 2023-02-07 · Relevance: HIGH · verify on Google Patents ↗

⚠ NOT IN FORCE — Expired - Fee Related (Google Patents structured data). This document itself poses no ongoing exposure; check family members via the link.

Potential overlap (AI reasoning):

- Claim 1/13 recite directly contacting non-metallic (dielectric) regions proximate to metallic pads on two substrates, then bonding the non-metallic regions and forming metal-to-metal pad contact — this broadly reads on the invention's copper-to-copper hybrid bonding via dielectric bonding surfaces surrounding embedded copper pads
- Claim 1/13 require heating the substrates in a range of about 100-250°C, which overlaps with the invention's post-bond anneal step causing copper expansion and fusion into continuous interconnects
- Claim 11/24 recite bonding the non-metallic regions at room temperature, overlapping with the invention's room-temperature bonding step prior to thermal processing
- Claims 3-5/16-18 recite exposing non-metallic regions to plasma (argon, nitrogen, or oxygen), overlapping with the invention's plasma surface activation of dielectric bonding surfaces
- Claims 6/19 recite polishing non-metallic regions to a surface roughness less than 15 angstroms, overlapping with the invention's CMP dielectric planarization step
- Claims 8-9/21-22 recite substantially planar metallic pad surfaces recessed below the non-metallic region's planar surface, which is a common hybrid-bonding pad topology overlapping with the invention's embedded copper pad structure
- The claims' generic 'metallic pads' language is broad enough to encompass the invention's specific copper pads, and 'non-metallic region' is broad enough to encompass the invention's dielectric material — broader claim language increases overlap risk

Appears to differ (AI reasoning):

- Claim 1 requires bonding the non-metallic regions 'without applying external pressure' and generating pad contact pressure as a direct result of that bonding — if the invention's process applies external mechanical/bonding pressure during the room-temperature bonding step, this specific mechanism may differ (though claim 13 does not have this 'without external pressure' limitation and may still overlap)

Note: This patent's claims are directed to substantially the same core process sequence as the invention: dielectric surface preparation (polishing/roughness control, optional plasma activation), direct contact bonding of dielectric surfaces surrounding metal pads, room-temperature bonding option, and a subsequent heating step (100-250°C) that establishes metal-to-metal pad contact/pressure — closely paralleling the invention's CMP planarization, plasma activation, room-temperature bonding, and post-bond anneal for copper expansion/fusion. Given the broad, generic claim language ('metallic pads,' 'non-metallic region'), there is substantial potential overlap with the invention's copper-to-copper hybrid bonding flow. This is an informational screening note only, not a legal or infringement conclusion; a full claims analysis with attention to claim differentiation between independent claims 1 and 13 (external pressure limitation) and prosecution history would be needed for a definitive assessment. ⚠ LEGAL STATUS (Google Patents): Expired - Fee Related — this document itself appears NOT in force and poses no ongoing exposure by itself; check family members via the link before relying on this.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The note does not flag sub-micron alignment control against the patent claims at all, but this is an omission rather than fabrication; claims do not recite alignment precision, so no overlap statement was made — acceptable.
- The distinguishing point about 'without applying external pressure' is properly caveated and not overstated, but the note fails to note that lack of a limitation in claim 13 (broader) increases risk rather than decreases it — it does mention claim 13 lacks this limitation, so it partially self-corrects, but the overall distinguishing section still frames this as a point favoring non-overlap without emphasizing that broader claim 13 is the greater risk, which is a mild wrong-direction framing.
- The statement that claims 8-9/21-22 pad recess topology is 'a common hybrid-bonding pad topology overlapping with the invention's embedded copper pad structure' is a slight interpretive stretch since the invention features describe embedded pads but do not explicitly state they are recessed below dielectric surface; this is a minor overstatement not directly supported by the invention feature list.
- The claim heating range 100-250°C is characterized as overlapping with 'post-bond anneal step causing copper expansion' — this is a reasonable inference but the invention features do not specify anneal temperature, so equating the two is a mild extrapolation beyond stated evidence.

3.14 US12218086B2 — Semiconductor package and method of manufacturing same

Assignee: Samsung Electronics Co Ltd · Published: 2025-02-04 · Status: Active · exp. 2043-08-05 · Relevance: HIGH · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 18 (dependent on claim 14) explicitly recites 'the first bonding pad and the second bonding pad are directly bonded by copper-to-copper bonding, and the first bonding insulating layer and the second bonding insulating layer are directly bonded by dielectric-to-dielectric bonding' — this generic Cu-Cu + dielectric-dielectric hybrid bonding language appears to read on the invention's copper-to-copper hybrid bonding interconnect and dielectric bonding surfaces.
- Claim 19 recites that bonding of the first and second structures 'includes at least one of die-to-die bonding, die-to-wafer bonding, and wafer-to-wafer bonding' — broadly encompasses the invention's wafer-to-wafer or die-to-wafer bonding configuration.
- Independent claims 1, 14, and 20 recite a 'first planarization process' and 'second planarization process' applied to the metallic material layer/insulating layer prior to bonding; these generic planarization steps could be read broadly enough to overlap with the invention's CMP-based dielectric/metal surface planarization step.
- Claim 14/20's overall structure of forming bonding pads then 'bonding the first structure and second structure, such that the first bonding structure is directly bonded to the second bonding structure' is a broad direct-bonding limitation that could encompass the invention's direct Cu-to-Cu DBI bonding without solder microbumps.

Appears to differ (AI reasoning):

- All independent claims (1, 14, 20) require preparation of 'a semiconductor structure including a semiconductor layer and a through-via penetrating through the semiconductor layer' — the invention description does not mention a through-via structure, so this claim element appears unmet.
- The independent claims require formation of a specific 'blocking layer' with a 'first portion covering the concaved portion' and 'second portion covering the non-concaved portion' of the metallic material layer, followed by a first planarization removing only the second portion — the invention's described CMP/plasma/anneal process does not include any blocking-layer step, so this specific limitation appears absent.
- The claims require a 'wet etching process' that removes the barrier layer on the insulating layer and forms a 'recessed portion below an upper surface of the metallic material layer' in the barrier layer — the invention's process (CMP, plasma activation, room-temperature bonding, post-bond anneal) does not describe any wet-etch-induced barrier recess formation.
- Claim 6 requires specific barrier layer thickness (about 100–200 nm) and recess depth (~300 nm or less); claim 5 requires the recess depth be ≥ barrier layer thickness — these quantitative barrier-layer/recess limitations are not addressed in the invention's described features.
- Claims 9–10 require an 'upper barrier layer' with a portion 'recessed upwardly' higher than the lower surface of the upper metallic material layer, and barrier layers of the two pads being 'spaced apart from each other' post-bonding — the invention's described Cu-to-Cu DBI/anneal expansion mechanism does not reference any barrier-layer recess or spacing structure, so this appears unaddressed.
- Claim 12 requires a three-layer insulating stack (first/second/third insulating layers with the second having a different material and the first extending along the through-via side surface) — no such layered insulating structure is described in the invention.

Note: This patent's claims are directed to a specific wafer-level metallization/patterning process (through-via, barrier layer, blocking layer, dual planarization, wet-etch recess formation) that culminates in hybrid (Cu-Cu + dielectric-dielectric) bonding of the resulting pads. The invention's described features (CMP planarization, plasma activation, room-temperature bonding, post-bond Cu anneal/expansion, sub-micron alignment) sit at a higher level of generality and overlap conceptually with the bonding-related claim language (claims 18–20), particularly the copper-to-copper/dielectric-to-dielectric bonding and die/wafer bonding modes. However, the independent claims impose numerous specific structural/process limitations (through-via, blocking layer, wet-etch-formed recessed barrier) not evidenced in the invention description, which appear to be missing elements. This is an informational screening note only; full claim charting against complete invention documentation and file history would be needed for a definitive assessment.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap analysis on claims 1, 14, and 20 planarization steps is somewhat overstated: these independent claims' 'first' and 'second' planarization processes are tightly bound to the blocking-layer/concave-portion structure, not generic CMP dielectric planarization as in the invention; equating them as 'could be read broadly enough to overlap' stretches the claim language beyond what the text supports.
- The note's distinguishing-points section repeatedly reasons that because the invention's described process lacks a feature recited in the claims (through-via, blocking layer, wet-etch recess, barrier layer dimensions, upper barrier layer recess/spacing, three-layer insulating stack), the claim 'appears unmet' or 'distinguishes' the invention from the patent. This is backwards FTO logic: for infringement purposes, extra limitations in the claim that the invention does not perform would mean the invention does NOT practice that specific narrow claim, which actually is correct direction for narrowing exposure — however, the note frames this as reducing risk from claims 1/14/20 while conceding overlap only with unclaimed dependent claims 18-19, which is roughly consistent. Still, framing 'the invention lacks X limitation therefore distinguishes' throughout as if it categorically reduces FTO risk without noting that these are narrow dependent-claim-heavy limitations tied to independent claims already requiring through-via/blocking layer (which the invention also lacks) is slightly redundant/repetitive rather than fabricated, but risks overstating the distinguishing strength since the core independent claims already fail

on the through-via/blocking-layer grounds alone, making the additional distinctions (claims 5,6,9,10,12) minor/duplicative rather than independently significant.

3.15 US12616050B2 — Bonded structure including a first microelectronic device direct hybrid bonded to a second microelectronic device

Assignee: Adeia Semiconductor Bonding Technologie, Adeia Semiconductor Bonding Technologies Inc · Published: 2026-04-28 · Status: Active · exp. 2040-04-14 · Relevance: HIGH · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1 (and independent claims 15, 24) recite a 'second microelectronic device direct hybrid bonded to [a] bonding surface without adhesive along a bond interface' — this broadly reads on the invention's copper-to-copper hybrid bonding/DBI approach that avoids solder microbumps.
- The claims recite conductive pad/via/buried-layer structures embedded in and surrounded by a dielectric structure, which overlaps with the invention's 'embedded copper pads' forming direct metallic interconnects.
- The patent's specification and claim structure (vertical stack of conductive layers with 'thermal expansion features designed to vertically expand the stack ... to make the direct metal-to-metal bonds') is directed to the same general phenomenon as the invention's post-bond anneal step causing copper pad expansion and fusion into continuous metallic interconnects — a close conceptual overlap, though claimed at the structural/geometric level rather than as a process step.
- Dependent claims 7-10, 18-19 reference nanotwinned copper, 111-oriented copper lattice planes, and nanotextured surfaces for low-temperature bonding — these relate to copper interconnect surface characteristics that could be present in (or a design choice for) a Cu-Cu DBI process like the invention's, warranting an equivalents-type caution even though the invention description does not specify such microstructural features.

Appears to differ (AI reasoning):

- Independent claims 1, 15, and 24 each require a specific three-tier conductive structure — a 'buried conductive layer' (first horizontal dimension), a 'buried conductive via portion' (smaller horizontal dimension, greater thickness-to-width ratio), and a 'conductive contact pad portion' with a horizontal dimension between the other two and a thickness >0.5 μm — connected by only a single via. The invention description does not describe this specific dimensional/geometric hierarchy for its embedded copper pads, so it is unclear whether this structural limitation is met.
- Claim 15 additionally requires a second, spaced-apart conductive contact pad portion over a 'nearest' second via — a specific multi-pad layout limitation not addressed in the invention description.
- The claims are structural/product claims defining precise horizontal-dimension and thickness relationships (e.g., third thickness 0.6-2 μm, first thickness 0.5-1.5 μm in dependent claims) with no recitation of the invention's process steps (CMP planarization, plasma activation, room-temperature bonding, sub-micron alignment) — since the invention's process steps are not required by the claims, they are not distinguishing, but the invention description also gives no indication that its embedded pads meet the claims' specific dimensional/via-count limitations.

Note: This patent's claims are structural (bonded-structure) claims specifying a detailed three-tier conductive layer/via/pad geometry with particular dimensional relationships, rather than process claims. The invention's core concept of copper-to-copper direct hybrid bonding without adhesive, embedded copper pads, and anneal-driven copper expansion/fusion shows conceptual and functional overlap with the claims' broad language on direct hybrid bonding without adhesive and expansion-based metal-to-metal bonding. However, the invention description lacks sufficient structural detail (via count, specific horizontal-dimension/thickness relationships, multi-pad layout) to assess whether it meets the more specific structural limitations recited in claims 1, 15, and 24. This is an informational screening note only, not a legal or infringement conclusion; a full technical/structural comparison against manufactured device cross-sections would be needed for a definitive assessment.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The distinguishing-points section explicitly acknowledges the correct FTO direction logic ('since the invention's process steps are not required by the claims, they are not distinguishing') but the overall framing of the bullet still lists process-step absence as part of a 'distinguishing points' section, which risks implying it weakens overlap; this is partially self-corrected but the placement is misleading and borderline wrong-direction in structure.
- The claim of overlap regarding dependent claims 7-10/18-19 (nanotwinned copper, 111-oriented lattice planes, nanotexture) as 'warranting an equivalents-type caution' is speculative — the invention description contains no mention of copper microstructure/crystal orientation, so asserting this as an overlap point (even hedged) goes beyond the provided invention features.
- The statement that the patent's 'vertical stack of conductive layers with thermal expansion features designed to vertically expand the stack' is in 'close conceptual overlap' with the invention's anneal-driven copper expansion is a reasonable inference from the abstract, but characterizing it as 'the same general phenomenon' is somewhat overstated given the patent ties this specifically to a precise recess-distance/geometric mechanism not described in the invention.

3.16 US12545010B2 — Directly bonded metal structures having oxide layers therein

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2026-02-10 · Status: Active · exp. 2043-11-13 · Relevance: HIGH · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1's overall architecture — a bonded structure with a first and second element each having nonconductive field regions directly bonded along a horizontal interface, and conductive features directly bonded to one another (hybrid bonding) — is broad and appears to read on the invention's copper-to-copper DBI hybrid bonding concept (dielectric-to-dielectric plus metal-to-metal bonding in a single interface).
- The invention's dielectric CMP planarization and plasma activation prior to bonding, followed by room-temperature joining, are process steps consistent with achieving the 'directly bonded' nonconductive field regions recited generically in claim 1; the claim does not specify how planarization/activation is achieved, so it is broad enough to encompass CMP/plasma-based surface preparation.
- The invention's post-bond anneal causing copper pads to expand and fuse into continuous metallic interconnects appears to overlap conceptually with claim 1's requirement that 'conductive features are directly bonded to one another,' since thermally-driven copper expansion/fusion is a known mechanism for achieving direct metal-metal bonding in hybrid bonding structures.
- Dependent claims 9 (inorganic dielectric field regions) and 17 (conductive feature as a contact pad) are broad/generic limitations that could also read on the invention's embedded copper pad and dielectric substrate configuration.

Appears to differ (AI reasoning):

- Claim 1 affirmatively requires that 'the first conductive feature comprises an oxide layer and conductive material vertically adjacent above and below the oxide layer, including between the oxide layer and the second conductive feature.' The invention description states that post-anneal copper pads 'expand and fuse into continuous metallic interconnects,' suggesting a continuous metal-to-metal junction rather than a structure with an embedded internal oxide layer sandwiched within/between the conductive features — this specific oxide-layer limitation does not appear to be addressed or present in the invention as described.
- Dependent claims 2, 3, 7, and 13 narrow the conductive feature material/oxide to aluminum, aluminum alloy (with copper/tantalum), or nickel with corresponding aluminum oxide/nickel oxide — these specific material limitations do not match the invention's copper-only embedded pad description, though this narrowing is only relevant to the dependent claims, not independent claim 1's broader oxide-layer requirement.

Note: This screening is based solely on the verbatim claims provided. Claim 1 is drafted broadly around a hybrid-bonded structure (dielectric-to-dielectric plus metal-to-metal bonding) and could potentially read on aspects of the invention's Cu-Cu DBI approach at a conceptual level; however, claim 1's specific structural requirement of an 'oxide layer' embedded within/adjacent to the conductive feature is a concrete limitation whose presence or absence in the invention cannot be confirmed from the provided invention description, which describes fused continuous copper interconnects without mention of an internal oxide layer. Whether the invention's copper interconnects incidentally contain a thin native/process-induced oxide layer (e.g., from CMP or plasma activation) would need factual/technical verification, as this could shift the analysis toward overlap under equivalents. Dependent claims narrow to aluminum/nickel-oxide chemistries, which appear less relevant to a pure copper system. This is an informational note only, not a legal or infringement conclusion.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap statement regarding CMP/plasma activation says 'the claim does not specify how planarization/activation is achieved, so it is broad enough to encompass CMP/plasma-based surface preparation' — this is wrong-direction-adjacent reasoning framed as overlap (broad/silent claim language supports overlap risk, which is correctly used here as an overlap point, but the note elsewhere uses similar silence to argue distinction, creating inconsistency).
- The distinguishing point about claim 1's oxide-layer requirement not being 'addressed or present' in the invention relies on the invention description being silent/not mentioning an oxide layer — using the invention's silence on a feature to distinguish is reasonable since the claim affirmatively requires a structural element (oxide layer) not described in the invention, so this is properly ranked (claim requires more than invention discloses), which is correct-direction reasoning, not fabrication.
- The note's final paragraph flags that the invention's copper might incidentally contain a native oxide layer, which appropriately hedges rather than fabricates, but slightly speculates beyond the provided invention features by introducing 'native/process-induced oxide' as a hypothetical not stated in the invention description.
- The statement that dependent claims 9 and 17 are 'broad/generic limitations that could also read on the invention's embedded copper pad and dielectric substrate configuration' is reasonable but slightly overstated since claim 17's 'contact pad' language is generic and not explicitly cross-referenced to copper in the abstract/claims, making the overlap claim somewhat speculative though not fabricated.

3.17 US20250006674A1 — Methods and structures for low temperature hybrid bonding

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2025-01-02 · Status: Pending · Relevance: HIGH · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1/29's requirement of a conductive feature (e.g., copper per claim 6/30) at least partially embedded in a dielectric material forming a bonding layer, with a bonding surface prepared for hybrid bonding, potentially reads on the invention's embedded copper pads used in copper-to-copper DBI hybrid bonding.
- Claim 29's step of directly bonding first dielectric material to second dielectric material of a second element potentially overlaps with the invention's room-temperature joining of dielectric bonding surfaces prior to thermal processing.
- Claim 29's post-bonding anneal step 'to complete a hybrid bond between the first conductive feature ... and a second conductive feature' potentially overlaps with the invention's post-bond anneal causing embedded copper pads to expand and fuse into continuous metallic interconnects, particularly given claim 30's copper/low-temperature (below ~250°C) annealing limitation.
- Claim 6/30 broadly covering copper as the conductive feature metal overlaps with the invention's copper-to-copper interconnect material.
- Claim 53's method of converting a top layer of an embedded conductive feature to an oxidized layer then to a metal layer, followed by bonding (per claim 1/29 framework), is a broader process step that could encompass a surface-treatment stage analogous to the invention's plasma

activation/preparation step, insofar as both involve preparing the conductive/dielectric bonding surface before joining.

Appears to differ (AI reasoning):

- Claims 1, 29, and 53 require providing a metal oxide layer over the conductive feature and chemically reducing it to a metal layer (with optional nanograin microstructure) as an affirmative process step; the invention as described uses plasma activation of dielectric surfaces rather than a metal-oxide-formation-and-reduction step on the conductive feature, so this specific oxide/reduction limitation does not appear to be present in the invention's described process.

Note: This patent's independent claims (1, 29, 53) are directed to a specific surface-preparation technique for hybrid bonding conductive features — forming a metal oxide layer over the conductive feature and chemically reducing it to a metal (optionally nanograin) layer before/during bonding — combined with dielectric-to-dielectric direct bonding and a subsequent anneal to complete the metal-to-metal bond, with copper and sub-250°C annealing specifically claimed in dependent claims. The invention's core copper-to-copper DBI process (embedded copper pads, CMP planarization, plasma activation, room-temperature bonding, post-bond anneal for copper fusion) shares significant conceptual overlap with the bonding/annealing framework of claims 29-30, particularly the anneal step to complete a hybrid bond and copper as the conductive material. However, the claims' specific and seemingly essential limitation of an oxide-formation-then-chemical-reduction step on the conductive feature is a distinct technical mechanism not evidently present in the invention's plasma-activation-based approach, which is the key basis for potential differentiation. This is an informational screening observation only, not a legal or infringement conclusion. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap statement regarding Claim 29's 'directly bonding first dielectric material to second dielectric material' being analogous to 'room-temperature joining' overstates support: claim 29 does not specify bonding temperature, so equating it to the invention's specifically room-temperature bonding step is an imprecise extension not directly supported by the claim text.
- The note's treatment of Claim 53 as potentially covering 'plasma activation/preparation' is speculative overstatement: claim 53 recites converting a conductive feature top layer to oxide then to metal, which is a materially different surface-preparation mechanism than plasma activation of dielectric surfaces; characterizing this as 'analogous' stretches the evidence.
- The distinguishing point reasons that because the invention lacks the claims' oxide-formation/reduction step, this differentiates it from the patent — but since claims 1/29/53 as independent claims are relatively narrow (already requiring the oxide/reduction step) rather than broad, this is not itself a wrong-direction FTO error; however, the note should more clearly acknowledge that the absence of a claimed narrowing feature in the invention argues non-infringement only if that limitation is indeed required, which the note does correctly frame — so this is a minor clarity point rather than a true logic error.

3.18 US11205635B2 — Low temperature hybrid bonding structures and manufacturing method thereof

Assignee: Individual · Published: 2021-12-21 · Status: Active · exp. 2040-07-22 · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1 recites bonding two dielectric layers of semiconductor structures together and then performing an anneal that turns copper features into a bulk-like continuous copper feature — broadly analogous to the invention's post-bond anneal that expands/fuses embedded copper pads into continuous metallic interconnects.
- Claim 4 recites that the two dielectric layers are flat and bonded together at room temperature, which potentially overlaps with the invention's dielectric planarization (CMP) and room-temperature bonding step.

- Claim 5/14 recite performing a CMP to planarize the copper fill layer to form the copper feature, which potentially overlaps with the invention's CMP-based dielectric/pad surface planarization prior to bonding.
- The overall claimed process of joining copper features between two dielectric-bonded semiconductor structures at low/room temperature followed by an anneal is broadly similar in outcome (continuous copper interconnect after anneal) to the invention's Cu-Cu DBI plus anneal expansion approach.

Appears to differ (AI reasoning):

- Claim 1 (and claim 7) require arranging a precursor/copper alloy containing an active metal (e.g., zinc, per claims 3/12) on a copper feature and performing a vacuum thermal dealloying step to self-organize a porous copper fill layer/pillar, which is then placed between the two copper features prior to anneal — the invention as described uses direct copper-to-copper contact via DBI without any intermediate alloy, active-metal component, dealloying step, or porous copper fill/pillar layer, so this claimed element appears absent from the invention.
- Claim 7 requires an adhesive layer (partially cured, then fully cured) on the dielectric surface of one structure and thermal compression bonding, which is a different bonding mechanism than the invention's plasma-activated direct dielectric bonding at room temperature; the invention does not appear to include an adhesive layer or thermal compression step.
- Dependent claims 8-10 require acetic acid immersion for copper-oxide reduction pretreatment and/or formic acid vapor environment during thermal compression bonding — these specific chemical pretreatment/environment limitations are not present in the invention's described plasma-activation approach.
- Claim 13 requires depositing separate first (pure copper) and second (active metal) layers followed by an anneal to convert them into the copper alloy — a layered alloy-formation process not present in the invention's direct Cu pad formation.

Note: This patent's claims center on a specific alloy/dealloying-based porous copper fill or pillar mechanism (with an active metal such as zinc) to achieve low-temperature bonding, which is a materially different technical approach from the invention's direct copper-to-copper hybrid bonding (DBI) using plasma-activated dielectric surfaces and post-bond thermal expansion of embedded copper pads without any intermediate alloy or dealloying step. Some generic process steps (CMP planarization, room-temperature dielectric bonding, post-bond anneal causing copper fusion) show potential overlap at a general level and should be reviewed further, particularly regarding whether the anneal-driven copper expansion in the invention could be viewed as functionally equivalent to the claimed alloy-to-bulk-copper conversion. This is an informational screening note only, not a legal or infringement conclusion.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap and distinguishing points are generally well-supported and accurately traced to claim text (claims 1, 4, 5/14, 7-10, 13), and the note correctly identifies the alloy/dealloying mechanism as a key distinguishing feature.
- However, the distinguishing points partly rely on the invention's DBI approach lacking an active-metal/dealloying step to conclude non-overlap, without adequately grappling with the fact that claim 1's core steps (bonding dielectric layers, then annealing copper features into bulk-like copper) are broad enough that the note's own overlap section flags them as potentially reading on the invention's post-bond anneal fusion step; the note does not clearly resolve whether claim 1 requires the porous fill layer as an essential limitation (which it does, per claim language 'arranging the porous copper fill layer between the two copper features'), so the distinguishing argument is basically correct but could be stated more precisely as claim-required-element-based rather than general approach-based.
- The note's final summary partially reasons that 'generic process steps... show potential overlap at a general level' which is appropriately hedged, but bundling CMP and room-temperature bonding as overlap risks overstating similarity, since claim 5/14 CMP is used to planarize the bulk copper fill (a manufacturing step forming the copper feature itself), not dielectric surface planarization prior to bonding as in the invention; this is a subtle mischaracterization of what the CMP step in the patent accomplishes.

3.19 US11742314B2 — Reliable hybrid bonded apparatus

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2023-08-29 · Status: Active · exp. 2041-03-22 · Relevance: HIGH · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1's core hybrid bonding sequence (preparing surface, plasma activating, then hybrid bonding to another surface via direct dielectric-to-dielectric and metal-to-metal bonding) broadly reads on the invention's plasma surface activation and room-temperature bonding steps, encompassing them as a species of the claimed genus
- Claim 2's preparation steps (forming cavities, forming conductive metal in cavities, planarizing the surface to provide smooth oxide surface and conductive metal recesses) potentially overlap with the invention's dielectric CMP planarization and embedded copper pad formation prior to bonding
- Claim 13's broader method (forming cavity, forming conductive metal, planarizing, rinsing, plasma activating, cleaning, then hybrid bonding to a second substrate's surface) overlaps with the invention's combination of CMP planarization, plasma activation, and copper-to-copper bonding for wafer-to-wafer/die-to-wafer/die-to-die configurations
- Claim 14's post-bond anneal at elevated temperature broadly overlaps with the invention's post-bond anneal step causing copper pad expansion and fusion into continuous metallic interconnects
- Claim 12's apparatus (directly bonded interface with low extraneous metal nanoparticle density) could overlap with the resulting bonded structure of the invention if such nanoparticle density is present, though this is incidental rather than a design feature of the invention as described

Appears to differ (AI reasoning):

- All independent claims (1 and 13) require an explicit post-plasma-activation cleaning step to remove metal particles/nanoparticles from the bonding surface; the invention description does not mention any such nanoparticle-removal cleaning step between plasma activation and bonding, which appears to be a required limitation the invention lacks as described
- Claim 12 requires a specific quantitative apparatus limitation (less than two extraneous metal nanoparticles per square micron on average), a measurable structural characteristic not described as part of the invention's feature set

Note: This patent's claims center on a nanoparticle-removal cleaning step performed after plasma activation but before bonding, which is the key limitation in independent claims 1 and 13. The invention's description (CMP planarization, plasma activation, room-temperature bonding, copper expansion anneal, sub-micron alignment) covers process steps that are broadly encompassed by the claim language for the surrounding hybrid bonding sequence (activation, direct dielectric and metal-to-metal bonding, post-bond anneal), suggesting potential overlap in the general bonding workflow. However, the claims' core novel and required element — cleaning to remove metal particles after activation — is not mentioned in the invention's disclosed features, which is the most significant gap; if the invention's actual process omits any post-activation particle-removal cleaning, dependent claims tied to that cleaning step (3-11, 15-21) would be even less relevant. This is an informational screening note only, not a legal opinion on infringement or freedom-to-operate; a full comparison would require the complete specification and any additional undisclosed process details of the invention.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The distinguishing point about claims 1 and 13 requiring a cleaning step that the invention lacks is reasoning in the correct direction for non-infringement analysis (a required limitation the accused process lacks would indeed avoid infringement), which is proper here since claims 1/13 are independent claims requiring that limitation — this is not wrong-direction reasoning, unlike a case where absence of a claim limitation is used to argue overlap. However the note's overlap section frames claim 1's sequence as 'encompassing them as a species of the claimed genus' while omitting that the claim also requires the cleaning step, which is inconsistent/overstated since the claim as a whole (including cleaning) is what must be compared, not just the activation/bonding portion in isolation.
- The claim 13 overlap statement omits that claim 13 also requires forming a cavity, conductive metal, planarizing, rinsing, AND the post-activation cleaning step as part of the single claimed method;

describing it as broadly overlapping while cleaning is absent from the invention is slightly misleading, though the note does clarify this later in the distinguishing section.

- The note's claim 12 overlap statement (nanoparticle density) is speculative ('could overlap... if such nanoparticle density is present') and is explicitly flagged by the note itself as incidental, which is appropriately hedged rather than fabricated.

3.20 US20250006679A1 — Conductive materials for direct bonding

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2025-01-02 · Status: Pending · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1's requirement of a first substrate and second substrate each with electrically conductive portions (e.g., copper per claim 5) and electrically insulative portions bonded together broadly overlaps with the invention's copper-pad/dielectric hybrid bonding structure.
- Claim 26's method of directly bonding first and second substrates without intervening adhesive, contacting conductive and insulative surface regions, broadly overlaps with the invention's direct (adhesive-free) copper-to-copper and dielectric bonding approach.
- Claim 31's planarizing step (e.g., CMP-like planarization of the conductive/oxide layer) potentially overlaps with the invention's CMP dielectric planarization step, though applied to a different conductive oxide layer.
- Claim 35's cleaning step prior to bonding and claim 36's post-contact annealing step broadly overlap with the invention's plasma activation/room-temperature bonding and post-bond anneal steps, as generic surface preparation and thermal treatment.
- Claim 5 lists copper as an option for the conductive portion, overlapping with the invention's embedded copper pads.

Appears to differ (AI reasoning):

- Claim 1 and its dependents require an 'interface layer' comprising 'at least one electrically conductive oxide material' (e.g., ITO or zinc oxide per claim 3) positioned between the first and second layers, forming first and second regions of electrical communication and isolation, respectively. The invention as described relies on direct copper-to-copper metallic fusion without an intervening electrically conductive oxide interface layer, so this required oxide-interface element appears absent from the invention.
- Claim 4's requirement of a first and second conductive oxide material each deposited on separate substrates and directly bonded to each other is a specific oxide-to-oxide bonding scheme not present in the invention's copper-to-copper DBI approach.
- Claims 7-16 require electrical isolation structures, gaps, or solid dielectric materials (e.g., silicon oxycarbonitride) within the conductive-oxide interface layer for hermetic sealing — these oxide-layer-specific isolation/sealing features are not described as present in the invention.
- Claim 26's method requires 'at least one of the first substrate and the second substrate' to include a patterned 'electrically conductive oxide layer' with isolated first/second regions — this conductive-oxide-layer patterning step is a required element not evidenced in the invention's process, which instead relies on plasma-activated dielectric surfaces and copper pad expansion during anneal.

Note: This patent's claims are centered on a distinct architectural element — an electrically conductive oxide interface layer (e.g., ITO, zinc oxide) situated between two substrates to mediate both conductive and insulative bonding regions — which is a materially different bonding mechanism from the invention's direct copper-to-copper metallic fusion via CMP planarization, plasma activation, and post-bond copper expansion. While broad claim language around direct bonding of substrates with conductive/insulative portions (claim 1, 26) and process steps like cleaning/annealing (claims 35-36) show conceptual overlap with hybrid bonding generally, the claims' consistent requirement of a conductive oxide interface layer is a limitation the invention as described does not appear to satisfy, unless the invention's copper pads themselves are characterized as or coated with a conductive oxide during processing (not indicated in the provided description). This is an informational screening note only, not a legal or infringement opinion. ℹ

PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap statement regarding Claim 1 is somewhat overstated: Claim 1 explicitly requires an 'interface layer' comprising 'at least one electrically conductive oxide material' between the first and second layers, which is a core structural limitation, not merely an incidental detail. Describing this as 'broadly overlapping' with copper-pad/dielectric hybrid bonding without emphasizing the required oxide interface layer understates how central that limitation is to the claim, though the note does correctly identify this as a distinguishing point later.
- The overlap statement for Claim 31 acknowledges the planarizing step is applied to 'a different conductive oxide layer' rather than dielectric, which appropriately hedges the comparison, but characterizing this as a meaningful 'overlap' is weak since the claimed planarization target (conductive oxide layer, per claim 26/31 context) differs materially from the invention's CMP of dielectric surfaces before bonding.
- The overlap statement for Claims 35-36 (cleaning and annealing) is somewhat generic/overstated — claim 36 simply recites 'annealing... after contacting,' with no mention of the specific copper-expansion mechanism or fusion outcome described in the invention; equating this generic anneal step to the invention's specific post-bond copper-expansion anneal is an overstatement of overlap.
- The distinguishing points reasoning is directionally sound in that it correctly notes the invention lacks the claimed conductive oxide interface layer (a genuine claim limitation absent from the invention), which is proper claim-scope analysis rather than wrong-direction reasoning.

3.21 US20240332227A1 — Semiconductor element with bonding layer having low-k dielectric material

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2024-10-03 · Status: Pending · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 26 recites a bonded structure formed from two elements each having a contact pad embedded in a dielectric layer, where the dielectric layers are directly bonded without adhesive and the contact pads are directly bonded to each other without adhesive — this broadly reads on the invention's Cu-to-Cu hybrid bonding interconnect concept (direct copper-to-copper bonding plus direct dielectric bonding without solder or adhesive).
- Claims 1, 3, 7 and 28 recite an interconnect structure with a contact pad/conductor 'forming part of a hybrid bonding surface,' which is a generic structural description that could encompass the invention's embedded copper pads used for hybrid bonding, regardless of the specific plasma-activation/anneal process used to form the bond.
- The claimed 'hybrid bonding surface' terminology and embedding of conductors in dielectric material generally overlaps with the invention's use of embedded copper pads on planarized dielectric surfaces as the bonding interface.

Appears to differ (AI reasoning):

- Independent claims 1, 7, and 28 all require a specific multi-layer dielectric barrier architecture (e.g., a first dielectric barrier layer between a first and second dielectric layer, a second conductive barrier layer, or a dielectric barrier layer with an angled/right-angle-turn portion between two dielectric layers) — the invention as described does not mention any such barrier layer structure, so this structural limitation appears unaddressed by the invention.
- Several claims require a 'low-k dielectric material' or 'plasma damage-free low-k dielectric material' as a specific composition of the second/low-k dielectric layer — the invention's description does not specify a low-k dielectric or a plasma-damage-free requirement for the dielectric itself (its plasma treatment is described as a surface activation step, not a material property tied to a barrier layer scheme).

- Claims 8–15 require specific via/underlying conductive feature arrangements with conductive barrier layers between the contact pad, via, and underlying feature — the invention's description centers on planarization, plasma activation, alignment, and post-bond anneal process steps rather than this claimed multi-tier conductor/barrier-layer stack, so this structural requirement is not addressed in the invention summary.
- The claims are structural/composition claims directed to the finished element (barrier layers, dielectric composition, layer geometry) rather than to the process steps (CMP planarization, plasma surface activation for room-temperature bonding, controlled post-bond anneal profile, sub-micron alignment) that form the core of the invention description; to the extent these process steps are not recited in the claims, they are not evaluated here, but the specific barrier-layer structural limitations noted above are elements the invention does not appear to include.

Note: This patent's claims are primarily structural/compositional, directed to a dielectric barrier layer architecture (including low-k dielectric material and conductive/dielectric barrier layers) surrounding contact pads in a hybrid-bonded interconnect, culminating in a bonded structure (claim 26) formed by direct dielectric-to-dielectric and pad-to-pad bonding without adhesive. The invention's Cu-Cu direct bond interconnect concept and use of a hybrid bonding surface show potential conceptual overlap with the broad 'hybrid bonding surface' and adhesive-free bonded structure language in claims 1, 3, 7, and 26. However, the claims' specific dielectric barrier layer geometry (e.g., right-angle turns, first/second barrier layers, low-k/plasma-damage-free dielectric composition) are structural limitations not described in the invention summary, which instead emphasizes process steps (planarization, plasma activation, alignment, anneal). Because claims text is provided in full and appears complete, this assessment is grounded in the verbatim claims; however, the invention description lacks structural/material detail (e.g., dielectric barrier layer composition) needed for a more precise comparison against the barrier-layer limitations, so some uncertainty remains regarding overlap versus difference at that level of detail. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The 'Distinguishing points' section reasons that because the invention description does not mention a barrier layer structure, low-k dielectric composition, or via/barrier stack, this 'distinguishes' the invention from the claims — but this is wrong-direction FTO logic: the claims' additional structural limitations (barrier layers, low-k composition) make the claims narrower/more specific, not broader, so their absence from the invention description does not by itself establish non-infringement; the note should be assessing whether the invention lacks these claimed elements (which would indeed avoid infringement of dependent/narrower claims), but the framing conflates 'not addressed in invention summary' with true absence, and repeatedly emphasizes this without acknowledging that independent claims 1, 7, and 28 still require these barrier-layer elements, meaning if the invention truly lacks them, that actually is a valid non-infringement argument for those claims — however the note's phrasing ('the invention as described does not mention...so this structural limitation appears unaddressed') is inherently uncertain reasoning based on absence of description rather than confirmed absence of feature, which is flagged as a minor overstatement of certainty.
- The claim overlap statements (claims 1,3,7,26,28) are reasonably supported by the verbatim claims text and are appropriately hedged with 'broadly reads on' and 'could encompass,' which is faithful.
- The note's final paragraph appropriately flags uncertainty about the invention lacking structural/material detail, which is a reasonable and faithful caveat rather than a fabrication.

3.22 US12506114B2 — Directly bonded metal structures having aluminum features and methods of preparing same

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2025-12-23 · Status: Active · exp. 2044-02-09 · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Independent claims 10, 11, 32, and 39 broadly recite a bonded structure formed by directly bonding a nonconductive field region to another nonconductive field region without adhesive, and directly bonding a conductive feature to another conductive feature without adhesive — this generic 'direct

hybrid bonding' architecture (dielectric-to-dielectric plus metal-to-metal bonding without solder/adhesive) overlaps conceptually with the invention's copper-to-copper DBI plus dielectric bonding scheme.

- Dependent claims 38, 44, and 47 allow the 'second portion' of the conductive feature to comprise copper, which could be read as encompassing a copper-containing bonding surface layer, showing some conceptual overlap with the invention's use of copper as the interconnect metal, though only as a secondary layer over a required aluminum first portion.

Appears to differ (AI reasoning):

- All independent claims (1, 10, 11, 16, 32, 39, 45) require the conductive/bonding feature to include a 'first portion comprising aluminum' (or an 'aluminum feature'), whereas the invention's interconnects are described as embedded copper pads with no aluminum-based first portion — this is a claim-required element the invention appears to lack.
- The claims require fluorine exposure/treatment of the aluminum surface (forming aluminum fluoride, aluminum fluoride oxide, etc.) to suppress aluminum oxide formation prior to bonding; the invention instead uses plasma activation of the dielectric surface for room-temperature bonding, with no indication of fluorine-based passivation of the metal pads themselves — a distinct surface-preparation chemistry not described in the invention.
- Several dependent claims (4, 5, 7, 13, 14, 18, 33, 40) require a specific two-portion aluminum feature with defined grain-size differences, recess depths (0.1–0.3 μm), and deposition temperature limits (<100°C) for the second portion — these structural/process limitations are specific to the patent's aluminum-based scheme and are not described as part of the invention's copper pad fabrication.
- Claims 11, 25, 26 require a fluorine concentration gradient at the bond interface and specific ppm limits for oxygen/nitrogen contamination — these compositional limitations tied to the fluorine-treated aluminum chemistry do not correspond to any described feature of the invention's copper-to-copper anneal/fusion process.

Note: This patent's claims center on a specific chemistry: an aluminum-based conductive feature (with an optional secondary portion, which may include copper) whose surface is treated with fluorine to suppress oxide formation prior to direct hybrid bonding. The invention, by contrast, describes a pure copper-to-copper DBI scheme using CMP planarization, plasma activation of dielectric surfaces, room-temperature bonding, and post-bond thermal anneal to fuse copper pads — with no aluminum content or fluorine-based surface treatment mentioned. While the overall 'dielectric-to-dielectric plus metal-to-metal direct bonding without adhesive' framework in the independent claims is broad enough to conceptually overlap with the invention's general DBI approach, the claims' explicit requirement of an aluminum first portion and associated fluorine surface chemistry represents a materially different technical implementation. This is a screening-level informational comparison, not a legal or infringement opinion; a full claim-chart analysis with expert review of the patent's specification (especially aluminum/copper hybrid embodiments) is recommended given partial conceptual overlap in the bonding architecture.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap statement citing claims 10, 11, 32, and 39 as 'broadly' reciting a generic direct hybrid bonding architecture is somewhat overstated — all these claims explicitly require an aluminum-containing feature (first portion comprising aluminum, or aluminum feature) as part of the bonding structure, not a generic conductive feature; the note's later distinguishing section correctly acknowledges this, creating some internal tension where the overlap section understates the aluminum requirement baked into the very same independent claims.
- The overlap statement regarding claims 38, 44, and 47 is reasonably supported (these claims do allow the second portion to comprise copper) but the characterization 'could be read as encompassing a copper-containing bonding surface layer' correctly notes it is secondary to a mandatory aluminum first portion, which is accurate and not fabricated.
- The distinguishing point about claims requiring an aluminum first portion is factually accurate per the claims, but framing it as a reason the invention is distinguished from the patent is directionally fine since it's a limiting requirement (narrowing) rather than the wrong-direction error of citing absence of a feature

in a claim as protective — this reasoning is used correctly here since the claims affirmatively require aluminum, which the invention lacks, so no wrong-direction issue found.

- The distinguishing point about fluorine-based surface treatment is well supported by claims 1, 9, 23, 24, 49, 50 and is accurately contrasted with the invention's plasma activation approach; no fabrication found.

3.23 US20240332231A1 — Direct hybrid bonding in topographic packages

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2024-10-03 · Status: Pending · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1 and claim 25 both recite 'direct hybrid bonded' die-to-substrate and die-to-die connections, a generic term that can encompass the invention's copper-to-copper DBI bonding technique without solder microbumps.
- The claims' use of broad, process-agnostic language ('direct hybrid bonded') does not exclude the invention's specific CMP planarization, plasma activation, room-temperature bonding, or anneal-driven copper expansion steps — these process details could fall within the scope of what is generically termed 'direct hybrid bonding' in the claims.
- Claim 3's reference to 'sintered conductive nanoparticles' as one electrical connection type suggests the patent contemplates metallic interconnect formation methods broadly, which may overlap conceptually with the invention's copper pad fusion via anneal, though the specific mechanism differs (sintering vs. thermal copper expansion/fusion).

Appears to differ (AI reasoning):

- Independent claim 1 requires a specific three-device-level stacked architecture (first die bonded to substrate, second die bonded to first die, third die bonded to top of second device level, with an added conductor electrically connecting the third die to the first die or substrate) — the invention as described is a generic two-substrate/wafer bonding process and does not appear to include this multi-tier die-stacking structure or the additional discrete conductor requirement.
- Independent claim 25 similarly requires an insulating material at least partially encapsulating first and second dies, a third die bonded to that insulating material, and a first conductor extending through the insulating material — these structural/encapsulation and via-conductor limitations are not described as part of the invention's bonding process.
- Several dependent claims require additional specific structures (interposer, redistribution layer, chiplet, protective coating, wire bonding pad, oxide plus polymer dielectric stack) that are not mentioned among the invention's described features; however, since these are dependent limitations, they are only relevant if the broader independent claim elements are met.

Note: This patent's claims are directed primarily to multi-tier die-stacking package architectures that employ 'direct hybrid bonding' as a connection technique, rather than to the specific wafer/die bonding process steps (CMP planarization, plasma activation, room-temperature joining, post-bond anneal-driven copper expansion, sub-micron alignment) that define the invention. There is conceptual overlap in that the claims' generic 'direct hybrid bonded' language could read on copper-to-copper DBI bonding methods like the invention's, but the independent claims additionally require specific multi-die stacked structural arrangements and conductors/encapsulation not described in the invention's feature set. This is an informational screening note only, not a legal or infringement opinion; a full claim-construction and prosecution-history review would be needed for a definitive assessment. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap analysis reasonably ties 'direct hybrid bonded' to the invention's copper-to-copper DBI bonding, which is supported by the claims text, but the note's characterization of it as a 'generic term' encompassing CMP planarization, plasma activation, room-temperature bonding, and anneal-driven copper expansion is speculative extrapolation beyond what the abstract/claims state — the claims never describe any process steps, so this is an overstatement though not fabrication.

- The distinguishing points correctly note that claim 1 and claim 25 require multi-tier die-stacking structures (three device levels, conductors, encapsulation) not described in the invention's features — this is factually supported.
- However, the note's overall framing that the patent claims are 'directed primarily to multi-tier die-stacking package architectures ... rather than to the specific wafer/die bonding process steps' and its listing of missing process details (CMP, plasma activation, room-temperature joining, anneal) as distinguishing points constitutes wrong-direction FTO reasoning: the claims not reciting these process limitations does not narrow them — it makes them broader and thus more likely to read on the invention if the structural elements are also met, not less dangerous. The note should flag this as increasing risk rather than treating the absence of these limitations as a point of distinction favoring non-infringement.
- The statement that dependent claims requiring interposer, redistribution layer, chiplet, protective coating, wire bonding pad, oxide+polymer dielectric stack are 'not mentioned among the invention's described features' is accurate, but the note appropriately caveats that dependent claims are narrowing and only relevant if independent claims are met, which is correct claim logic — not an issue.
- The comparison of claim 3's 'sintered conductive nanoparticles' to the invention's copper pad fusion via anneal is speculative but appropriately hedged with 'may overlap conceptually' and 'specific mechanism differs,' which is faithful to the evidence's ambiguity rather than fabrication.

3.24 US20250316625A1 — Semiconductor packages including mixed bond types and methods of forming the same

Assignee: Taiwan Semiconductor Manufacturing Co TSMC Ltd · Published: 2025-10-09 · Status: Pending · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claims 1, 8, 15 require 'direct bonding' forming both a dielectric-to-dielectric bond and a metal-to-metal bond between a die and a redistribution structure — this broad, generic claim language for metal-to-metal direct bonding could encompass the invention's copper-to-copper hybrid bonding (DBI) interconnect scheme, including its underlying dielectric bonding and CMP/plasma-activation/room-temperature/anneal process steps, since the claims do not limit the metal-to-metal bond to any particular metal or process technique.
- The claimed 'dielectric-to-dielectric bond' element is broad enough to read on the invention's CMP-planarized, plasma-activated dielectric surfaces bonded at room temperature, as no specific surface preparation method is excluded by the claim language.
- The claimed post-bond thermal/encapsulation processing (e.g., forming encapsulant, planarizing) is generic and does not exclude a controlled anneal step causing copper pad expansion/fusion, so the invention's anneal step is not distinguished from the claim's broad process flow.

Appears to differ (AI reasoning):

- Every independent claim (1, 8, 15) additionally REQUIRES a second die attached by 'solder bonding' (with associated under-bump metallization/solder joints) alongside the direct-bonded die — i.e., a mixed bond-type package. The invention as described appears to be a purely copper-to-copper hybrid-bonded interconnect scheme without solder microbumps, so it appears to lack this required solder-bonded second-die element unless a solder-bonded component is separately present in the overall product.
- The claims require a redistribution structure/interposer or interface die architecture with a first and second bonding surface pairing a direct-bonded die and a solder-bonded die in a single package; the invention's described features (alignment, CMP, plasma activation, anneal) pertain only to the bonding interface itself and do not indicate this specific mixed-bond package architecture.

Note: This patent's claims center on a package architecture combining direct (hybrid) bonding for one die with solder bonding for a second die on the same redistribution/interposer structure. The invention's disclosed hybrid-bonding process features (Cu-Cu DBI, CMP, plasma activation, room-temperature bonding, anneal-induced Cu expansion, sub-micron alignment) could fall within the broad 'direct bonding'/'metal-to-metal bond'/'dielectric-to-dielectric bond' language of independent claims 1, 8, and 15, representing potential overlap on the bonding technology itself. However, each independent claim also

mandates a solder-bonded second die as a structural limitation, which is not indicated as part of the invention's described interconnect scheme — this is a potential distinguishing element depending on whether the invention's actual end product also incorporates solder-bonded components elsewhere. Claims text was provided and reviewed in full; assessment is based solely on that text. This is an informational screening note, not a legal or infringement opinion. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap analysis is reasonable and traceable to claim language (direct bonding, dielectric-to-dielectric bond, metal-to-metal bond in claims 1, 8, 15), but the distinguishing points rely on the invention lacking the claimed solder-bonded second die — this is correctly noted as a limitation that narrows the claim, which is directionally correct reasoning (narrower claim requiring an additional element is a valid distinguishing point since the invention as described doesn't include it), so this part is not wrong-direction.
- The statement that 'the claimed post-bond thermal/encapsulation processing... is generic and does not exclude a controlled anneal step' is an overlap claim reasoning from absence of exclusion, which risks overstatement since the claims don't affirmatively recite any anneal step causing copper expansion; this is a weak but not fabricated inference from claim breadth.
- The note's characterization that CMP/plasma-activation/room-temperature/anneal process steps could be 'encompassed' by the broad claim language is a reasonable but speculative extrapolation — the claims recite the resulting bond types, not the process steps themselves, so equating process-based invention features with a product-by-process-style claim overlap is somewhat overstated without more support.

3.25 US12557615B2 — Methods for bonding semiconductor elements

Assignee: Adeia Semiconductor Technologies LLC · Published: 2026-02-17 · Status: Active · exp. 2044-05-25 · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1/17/23 require forming a plurality of conductive contacts in a dielectric bonding layer and directly hybrid bonding that layer (and, per claim 11, the embedded contacts of both elements) to a second element without an intervening adhesive — this generic hybrid-bonding-without-adhesive limitation is broad enough to potentially read on the invention's copper-to-copper DBI interconnect formed by embedded copper pads on two substrates.
- Claim 6 recites polishing the dielectric bonding layer prior to bonding, which potentially overlaps with the invention's CMP planarization step for dielectric surface flatness.
- Claim 7 recites activating the dielectric bonding layer after polishing, which potentially overlaps with the invention's plasma surface activation step enabling room-temperature bonding.
- Claim 21 specifies activation via nitrogen plasma exposure, a species of plasma activation that potentially overlaps with the invention's plasma-activation step (equivalents caution as invention does not specify plasma chemistry).
- Claim 13 (additional anneal after bonding to increase bond strength) and claim 12 (anneal to densify contacts) are directed to post-bond thermal processing that potentially overlaps with the invention's post-bond anneal step causing copper expansion/fusion, though the claimed anneal is specifically a 'microwave anneal' whereas the invention's anneal mechanism is not specified as microwave-based (equivalents caution).

Appears to differ (AI reasoning):

- Independent claims 1, 17, and 23 all require 'microwave annealing' of the dielectric bonding layer (exposure to microwave radiation, e.g., 2–15 GHz per claim 10) performed before forming the conductive contacts and before bonding; the invention's described process (CMP planarization + plasma activation + room-temperature bonding) does not indicate use of microwave radiation for annealing the dielectric layer, so this specific claim requirement appears absent from the invention as described.

- Claim 2/17 require depositing the dielectric bonding layer at a first (higher) temperature and then microwave annealing it at a second (lower) temperature in a defined sequence tied to deposition — the invention's disclosed steps do not describe a two-temperature deposition/microwave-anneal sequence for the dielectric layer.
- Claim 14 requires providing TSVs exposed through a back side and microwave annealing a dielectric layer over them to densify it; the invention's feature list does not mention TSVs or backside dielectric densification, so this additional claim element appears unmet.
- Claim 9/10 require the microwave annealing to use a plurality of different microwave frequencies or frequencies specifically in the 2–15 GHz range — absent any microwave step in the invention, these narrower limitations also appear unmet.

Note: This is an informational screening note only, not a legal or infringement opinion. The patent's independent claims are structured around a microwave-annealing step applied to the dielectric bonding layer prior to conductive-contact formation and hybrid bonding — a specific processing technology not evidenced in the invention description, which instead relies on CMP planarization, plasma activation, room-temperature joining, and a post-bond thermal anneal for copper expansion. Several dependent-claim elements (polishing, plasma/nitrogen-plasma activation, post-bond anneal to increase bond strength, direct bonding of embedded contacts without adhesive) use broad or generic language that could potentially encompass analogous invention steps, warranting closer review of the actual anneal mechanism and process sequence used in the invention, ideally with full specification and file history review.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The note claims 'the invention's disclosed steps do not describe a two-temperature deposition/microwave-anneal sequence' and lists absence of microwave annealing as a distinguishing point for independent claims 1/17/23 — but since claims 1/17/23 are independent claims that would need to be met in their entirety for infringement, correctly noting missing elements (microwave annealing) as absent from the invention is valid non-infringement reasoning, not wrong-direction; however the note's framing throughout emphasizes narrower dependent-claim limitations (claims 9,10,14) being 'additional' and 'narrower' and their absence being distinguishing, which is correct since dependent claims add limitations. This part is faithful reasoning.
- The statement about claim 21 (nitrogen plasma) noting 'invention does not specify plasma chemistry' and treating this as an equivalents caution rather than a clean distinction is reasonable, but the note does not commit a wrong-direction error there since claim 21 is a dependent narrowing claim.
- Overall the note is largely faithful to claim text and invention features; the potential minor issue is that the note repeatedly treats absence of narrower dependent claim features (TSVs, frequency ranges) as strengthening the distinguishing case, which is appropriate since dependent claims narrow scope, but it could better clarify that the broader independent claims are the primary infringement risk, and the extensive 'distinguishing' discussion of narrow dependent claims could understate that risk to a reader focused only on independent claims.

3.26 US11121121B2 — 3D semiconductor device and structure

Assignee: Monolithic 3D Inc · Published: 2021-09-14 · Status: Active · exp. 2039-09-02 · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claims 4, 11, and 17 recite that levels are 'bonded... with hybrid bonding,' a generic term broad enough to encompass the invention's copper-to-copper hybrid bonding/DBI process, including dielectric planarization, plasma activation, room-temperature bonding, and post-bond anneal steps used to form the bonded interconnect
- The independent claims (1, 8, 15) describe multi-level 3D semiconductor devices with logic and memory levels directly bonded/stacked, which is the general device context in which the invention's hybrid bonding interconnect technology would be applied

Appears to differ (AI reasoning):

- The independent claims (1, 8, 15) require specific circuit-level architecture (single crystal silicon logic level, memory arrays, RF circuit level, specific interconnection topology between logic circuits via RF circuits) that is not part of the invention's described bonding-process features, but these are additional device-level requirements the invention's process would need to fit rather than differences in the bonding technology itself
- Claims requiring channels for fluid cooling (2, 8) or specific die dimensions >40 mm (3, 10, 15) impose limitations unrelated to the described interconnect/bonding features and are not addressed by the invention description

Note: This patent's claims are directed to a 3D device architecture (multi-level logic/memory/RF stacking) that generically invokes 'hybrid bonding' (claims 4, 11, 17) without specifying implementation details (no explicit recitation of copper pad expansion via anneal, plasma activation, CMP planarization, or sub-micron alignment). Because 'hybrid bonding' is broad and could encompass copper-to-copper DBI bonding as one known implementation, there is potential overlap on the bonding-method limitation if the invention's process were used to join levels in a device meeting the other architectural limitations (multi-level logic/memory/RF structure). However, the claims' primary distinguishing subject matter is the specific 3D circuit architecture, not the bonding process mechanics, so overlap is dependent on how narrowly 'hybrid bonding' is construed and whether the invention is deployed in a device meeting the other structural limitations. This is an informational screening note only, not a legal opinion.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The note's framing that lack of explicit recitation of CMP planarization, plasma activation, anneal, and sub-micron alignment in the claims is a 'distinguishing point' is wrong-direction reasoning: broader/generic claim language ('hybrid bonding' without limiting implementation details) is more likely to read onto the invention, not less, so this should increase FTO risk rather than serve as a distinguishing factor. The note partially acknowledges this nuance in the final paragraph, but the bullet list still presents the absence of these limitations as if it were a distinguishing point, which is inconsistent and could mislead.
- The statement that claims 2/8 (fluid cooling channels) and claims 3/10/15 (die dimension >40mm) are 'not addressed by the invention description' is accurate as a lack of feature overlap, but since these are dependent claims adding narrowing limitations (not present in independent claims 1/8/15), citing them as distinguishing has limited relevance to overall FTO risk from the broader independent claims and could overstate the degree of distinction achieved.

3.27 US11621249B2 — 3D semiconductor device and structure

Assignee: Monolithic 3D Inc · Published: 2023-04-04 · Status: Active · exp. 2039-09-02 · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Dependent claims 4, 11, and 16 recite that 'said first level is bonded to said second level with hybrid bonding' — this is a broad/generic term for hybrid bonding that could encompass the invention's copper-to-copper direct bond interconnect (DBI) approach, since Cu-Cu hybrid bonding is a species of the claimed genus 'hybrid bonding'.
- The invention's room-temperature bonding, CMP planarization, plasma activation, and post-bond anneal are standard process steps used to achieve 'hybrid bonding' as generically claimed; to the extent the claims' hybrid-bonding limitation is read broadly, these process details would fall within its scope as an equivalent implementation.

Appears to differ (AI reasoning):

- Independent claims 1, 8, and 14 all require a specific 3D device architecture — a first level of single crystal silicon with logic circuits/transistors having an area greater than 1,000 mm2 — which is not described as part of the invention (the invention is characterized as a bonding/interconnect process, not a full logic-plus-memory/RF device with a defined silicon area).
- All three independent claims require a second level (memory arrays, RF circuits, or transistors respectively) disposed above the first level; the invention description does not specify such a multi-level logic/memory or logic/RF device architecture.

- All three independent claims require a 'thermal isolation layer disposed between said first level and said second level' providing a greater than 20°C differential temperature during nominal operation — the invention's feature list contains no thermal isolation layer or associated temperature-differential functionality, so this claim limitation appears unmet.
- The hybrid-bonding limitation in claims 4, 11, and 16 is only a dependent limitation layered onto the independent claims' specific area/thermal-isolation/multi-level architecture; absent those base elements, the dependent claims as a whole would not be reached regardless of the bonding-method overlap noted above.

Note: This patent's claims are directed to a large-area (>1,000 mm2 single crystal silicon), multi-level 3D device architecture combining logic with memory/RF/transistor layers and a specific thermal-isolation-layer limitation (>20°C differential) — a device-level architecture claim set, not a claim to the copper-to-copper hybrid bonding process itself. The only point of potential overlap is the generic 'hybrid bonding' term in dependent claims 4, 11, and 16, which could broadly encompass Cu-Cu DBI bonding as one implementation. However, because these are dependent claims, overlap is only relevant if the invention (or a downstream product) also embodies the independent claims' specific silicon-area, multi-level, and thermal-isolation-layer requirements, which are not indicated in the provided invention features. This assessment is based solely on the verbatim claims text provided and should not be treated as a legal or FTO conclusion.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The distinguishing points list the absence of the invention's process features (CMP planarization, plasma activation, room-temperature bonding, post-bond anneal) or absence of a full device architecture as reasons the invention differs from the claims; however, since claims 1/8/14 are independent claims that do NOT recite these specific bonding process steps at all, arguing that the invention lacks additional described architecture (large-area silicon, thermal isolation layer) is valid, but framing the dependent hybrid-bonding claims as narrowed/less relevant because the invention doesn't also embody the independent claims' broader architecture inverts the standard infringement logic to some extent — dependent claims are narrower, so the analysis correctly notes overlap must reach the independent claim limitations first, which is correct direction; however the note's earlier statement that CMP/plasma/anneal details 'would fall within scope as an equivalent implementation' of the generic hybrid bonding term is somewhat speculative and not clearly grounded in the claim text, which never describes bonding process steps, so equating unclaimed process specifics as automatically covered by the generic term overstates support.
- The claim of overlap for dependent claims 4/11/16 is appropriately caveated but the note's final summary continues to imply meaningful potential overlap ('point of potential overlap') despite acknowledging the independent claims' unmet limitations, which slightly overstates the practical relevance of the dependent-claim overlap given the surrounding unmet independent limitations.

3.28 US12324268B2 — Image sensor device

Assignee: Adeia Semiconductor Technologies LLC · Published: 2025-06-03 · Status: Active · exp. 2035-11-18 · Relevance: HIGH · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claims 1, 11, and 23 broadly recite dielectric layers of two die/wafers 'directly bonded to one another without any adhesive' together with metallic pads 'directly bonded to one another for electrical connectivity' — this generic dielectric-to-dielectric plus pad-to-pad direct bonding scheme reads on the invention's copper-to-copper hybrid bonding interconnect and dielectric bonding surfaces.
- Dependent claims 7, 17, and 25 specifically recite 'copper-to-copper bonding' between the metallic pads, directly overlapping with the invention's copper-to-copper DBI interconnect feature.
- Dependent claims 6, 16, and 24 recite 'oxide-to-oxide bonding' of the dielectric layers, which overlaps with the invention's dielectric surface bonding step (though the claims do not specify CMP planarization or plasma activation, the broad 'directly bonded' language could encompass surfaces prepared by such methods).

- The claims' requirement that dielectric and metallic surfaces be bonded 'without any adhesive' is consistent with (and broader than) the invention's room-temperature direct bonding step preceding anneal-induced copper fusion.

Appears to differ (AI reasoning):

- Claims 1, 11, and 23 require a specific device architecture — an 'image sensor die' with 'at least one light sensing element' bonded to a 'processor die' — whereas the invention as described is a generic wafer-to-wafer/die-to-wafer hybrid bonding process not limited to image sensor or processor die applications; the claims' structural requirement of these specific die types is not addressed in the invention description.
- Claim 1 additionally requires 'insulating material' extending along substantially the entire side surface of the processor die (or bulk semiconductor layer in claim 11, or side surfaces generally in claim 23), a specific packaging-level structural limitation (e.g., molding, epoxy, or coating per claims 3, 8, 9, 13, 18, 19, 26) that is not present in the invention's described features, which focus on the bonding process itself rather than side-surface encapsulation.
- Claims 4, 5, 14, and 15 require conductive pathways (plated pillars/vias) through the insulating material and a redistribution layer, structural elements not mentioned in the invention's feature list.
- Claim 28 requires a diced sidewall extending from the image sensor die's back side through at least the processor die's second dielectric layer — a specific dicing/structural configuration not described in the invention.
- The claims are drawn to a resulting bonded device structure (an apparatus), while several invention features (CMP planarization, plasma activation, room-temperature bonding step, post-bond anneal profile, sub-micron alignment control) describe process steps not recited as structural limitations in the claims — process specifics like CMP, plasma activation, anneal profile, and alignment precision are absent from the claim language, though this does not by itself avoid the broader structural bonding limitations noted as overlaps.

Note: This patent's independent claims (1, 11, 23) center on a resulting image sensor/processor die structure joined via direct dielectric bonding and direct copper-to-copper (or generally metallic) pad bonding without adhesive — core concepts closely aligned with the invention's Cu-Cu hybrid bonding and dielectric bonding features, producing high potential overlap on the fundamental bonding mechanism. However, the claims are narrowed by device-specific structural context (image sensor die + processor die, side-surface insulating material/molding/epoxy, conductive pathways, dicing configuration) that is not clearly present in the invention's generic process description, and the claims do not recite the invention's specific process steps (CMP, plasma activation, anneal profile, sub-micron alignment) as limitations, meaning those process details are largely irrelevant to claim scope. This is an informational screening note only, not a legal or infringement opinion.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The distinguishing point regarding CMP/plasma activation/anneal/alignment states that because the claims do not recite these process limitations, the invention's process details are 'largely irrelevant to claim scope' or serve as a distinguishing factor — this is wrong-direction reasoning, since the claims being silent on these process steps means the claims are broader and could still read on a product made via such a process; the absence of these limitations makes the claim more dangerous (more likely to read on the invention), not less, so citing this as a distinguishing point is logically backwards.
- The final summary paragraph repeats this wrong-direction reasoning by framing the claims' non-recitation of CMP, plasma activation, anneal profile, and alignment precision as a narrowing/distinguishing factor, which mischaracterizes FTO risk logic.
- The claim that the invention 'is a generic wafer-to-wafer/die-to-wafer hybrid bonding process not limited to image sensor or processor die applications' is a reasonable inference from the invention feature list, which indeed does not mention image sensor or processor dies, so this is faithful, though it should be noted the distinguishing weight placed on this is legitimate since it is a genuine structural claim limitation (unlike the process-step point).

3.29 US20250266400A1 — Electrical redundancy for bonded structures

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2025-08-21 · Status: Pending · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 2 (and 19, 25) broadly recites a bonded structure with a first element having metal pads directly bonded to a second element's metal pads, and dielectric field regions directly bonded without adhesive (claim 7) — this generic direct-bond structure could read on the invention's copper-to-copper hybrid bonding interconnect and its planarized dielectric surfaces bonded together
- Claim 6 requires direct bonding of metal pads 'without an intervening adhesive,' which overlaps with the invention's solder-free copper-to-copper DBI approach
- Claim 7's directly bonded dielectric field regions without adhesive potentially overlaps with the invention's CMP-planarized and plasma-activated dielectric surfaces prior to bonding, as the claim does not exclude such surface preparation and broadly covers the resulting bonded dielectric interface

Appears to differ (AI reasoning):

- Independent claims 2, 19, and 25 center on redundancy/spacing schemes among metal pads (electrically redundant/non-redundant pads, specific spacing ranges relative to pitch) — the invention as described does not mention any redundant pad architecture or specified inter-pad spacing ratios, so claims requiring these redundancy limitations may not be met by the invention's disclosed features
- Claims 3-5, 9, 14-17, 20-21, 27, 29-30 require specific numerical spacing/pitch ratios between pads for redundancy purposes, which are not addressed in the invention description
- Claim 24 requires a selectively-enabled shorting circuit between pads — no such circuit is described in the invention
- Claims 10-13, 18, 22-23, 28, 31 add further redundancy-related circuitry/trace/pad-count limitations not present in the invention's described features

Note: This patent family concerns electrical redundancy schemes for hybrid/direct-bonded structures (redundant contact pads, spacing ratios, shorting circuits) rather than the core hybrid bonding process steps (CMP planarization, plasma activation, room-temperature bonding, anneal-induced copper expansion, sub-micron alignment) that define the invention. The invention's foundational direct-bond/copper-fusion process appears broadly consistent with the generic 'direct bonding' language in claims 2, 6, 7, 19, and 25, warranting an overlap flag, but the claims' distinguishing subject matter — pad redundancy and spacing schemes — is not addressed by the invention as described. This is an informational screening note only; a full comparison would require reviewing the complete specification and any related patents in this family covering the base hybrid bonding process (e.g., parent DBI patents) not included here. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- Distinguishing point relying on independent claims 2, 19, 25 requiring redundancy/spacing schemes 'not mentioned' in the invention is a wrong-direction inference in one sense: since these are independent claims defining the broadest scope of what would infringe, correctly noting the invention lacks those elements is actually valid non-infringement reasoning (claim requires X, invention has no X supports distinguishing) — this is fine, not an error. However, the claim 7 overlap statement asserting the claim 'does not exclude' CMP/plasma surface prep and 'broadly covers' the resulting interface is speculative overstatement not directly grounded in the claim language, which only requires directly bonded dielectric regions without adhesive and says nothing explicit about planarization or plasma activation methods being covered.
- The note's claim 6 overlap statement is reasonably supported, but characburizing the invention's plasma activation and room-temperature bonding process steps as being covered by claim 6/7's structural 'without adhesive' limitation somewhat conflates process claims-style features (plasma activation, anneal

profile, alignment precision) with the patent's purely structural claim language, slightly overstating overlap since the patent claims do not recite plasma activation, room temperature bonding, or anneal-induced expansion at all.

- The summary characterization that the patent 'concerns electrical redundancy schemes... rather than the core hybrid bonding process steps' is well supported by the claims, but the note simultaneously flags overlap based on generic direct-bonding language in the same claims, which is somewhat internally tense (overlap claimed on the generic parts while emphasizing the redundancy focus as distinguishing) — this is a minor imprecision rather than fabrication.

3.30 US20240178256A1 — Image sensor device

Assignee: Adeia Semiconductor Technologies LLC · Published: 2024-05-30 · Status: Pending · Relevance: HIGH · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 2/10/15 recite a processor die directly bonded to a sensor die without intervening adhesive — this genus of direct dielectric bonding reads on the invention's copper-to-copper hybrid bonding structure formed via room-temperature bonding and anneal.
- Claim 3/16 recite direct hybrid bonds between processor and sensor die, which corresponds broadly to the invention's copper-to-copper DBI interconnect concept.
- Claim 4/17 (first/second dielectric layers directly bonded) overlaps with the invention's dielectric surface bonding step, though the claim does not specify CMP planarization or plasma activation, it is broad enough to encompass any method of achieving direct dielectric bonding, including the invention's approach.
- Claim 5/10/17 (first and second metallic pads with direct hybrid bonds formed between them) overlaps with the invention's embedded copper pads forming direct metallic interconnects.
- Claim 7/12/19 (metallic pads comprising copper material) overlaps with the invention's copper-to-copper interconnect material choice.
- Claim 6/11/18 (dielectric layers comprising oxide material) is broad enough to encompass the invention's planarized dielectric surfaces, which are typically oxide-based in CMP/hybrid bonding flows.

Appears to differ (AI reasoning):

- Claims are limited to an 'image sensor device' structure — the sensor die must comprise an image sensor (claims 2, 10, 15) and in several dependent claims a back side illuminated image sensor (claims 8, 13, 20); the invention as described is a generic hybrid bonding interconnect process/structure with no recited image sensor functionality, so claims requiring an image sensor element may not be met unless the invention is embodied in an image sensor context.
- Claims require the sensor die to originate 'from a reconstituted wafer' (claims 2, 10, 15); the invention's description of wafer-to-wafer or die-to-wafer bonding does not specify a reconstituted wafer origin, which could be a missing structural limitation if the invention's substrates are not reconstituted wafers.
- Claims 9/14/21 require a specific orientation — an active surface of the image sensor opposite a second surface bonded to the processor die; the invention does not describe this back-side bonding orientation relative to an active sensor surface.

Note: This patent's claims are directed to image sensor devices formed via direct/hybrid copper-to-copper dielectric bonding between a sensor die (from a reconstituted wafer) and a processor die. The core bonding structure (dielectric-to-dielectric direct bond plus copper-to-copper metallic pad interconnects) shows significant potential overlap with the invention's copper-to-copper hybrid bonding interconnect features, particularly claims 5, 7, 10, 12, 17, and 19, which are broadly drafted and do not exclude CMP planarization, plasma activation, room-temperature bonding, post-bond anneal, or sub-micron alignment — process details not recited in the claims cannot be relied upon to distinguish, since the claims' structural language (direct bonds, metallic pads, copper material) may generically encompass the resulting structure regardless of process specifics. However, all independent claims are limited to an

'image sensor device' with a sensor die 'from a reconstituted wafer,' which are structural/context limitations not evidently present in the invention as described (a general hybrid bonding interconnect technology). This is an informational screening note only, not a legal or infringement opinion; a full comparison would require knowing whether the invention is applied specifically to image sensor/processor die stacks originating from reconstituted wafers. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap statement for claim 4/17 explicitly notes 'the claim does not specify CMP planarization or plasma activation' as a basis for finding it 'broad enough to encompass' the invention — this is correctly reasoned as an overlap risk (broader claim = more dangerous), but the note's own summary paragraph then reuses similar language ('process details not recited in the claims cannot be relied upon to distinguish') to correctly avoid the wrong-direction trap; however the initial bullet phrasing risks being misread as treating the absence of limitations as a distinguishing feature rather than an overlap risk, so it is imprecise/ambiguous in framing.
- The claim 6/11/18 overlap statement asserts dielectric layers 'comprising oxide material' are 'typically oxide-based in CMP/hybrid bonding flows' — this is an inference about typical practice not explicitly stated in the invention features (which only mention 'dielectric surfaces' without specifying oxide composition), so this is a mild overstatement beyond the provided evidence.
- The distinguishing point about 'reconstituted wafer' origin is reasoned correctly as a potential structural limitation absent from the invention, which is appropriate direction (narrower claim element not met by invention descriptor) — no issue here, but it assumes the invention's substrates are wafers/dies in a manner that may or may not qualify as 'reconstituted,' which is speculative since the invention features do not address wafer sourcing at all; this speculation is acknowledged with hedging language ('could be a missing limitation... if'), which is appropriately cautious.

3.31 US20250300135A1 — Offset pads over tsv

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2025-09-25 · Status: Pending · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claims 2, 10, and 15 recite direct bonding of first and second contact pads without an intervening adhesive, which is a broad structural claim to copper-to-copper (or metal-to-metal) hybrid bonding that could encompass the invention's Cu-Cu DBI interconnect structure
- Claims 10 and 14-15 recite 'hybrid bonded' surfaces including dielectric-to-dielectric direct bonding combined with contact pad-to-contact pad bonding, which broadly overlaps with the invention's combination of planarized dielectric bonding surfaces and embedded copper pad interconnects
- The claimed 'first contact pad at least partially embedded in the first dielectric layer and extending to the first dielectric surface' (claim 10) is broad language that could read on the invention's embedded copper pads at a planarized dielectric surface
- Claim 3-5 and 8-9's dielectric layer limitations at the bonding surface are generic enough to potentially cover the invention's CMP-planarized dielectric surfaces prior to bonding

Appears to differ (AI reasoning):

- All independent claims (2, 10, 15) require a through-substrate via (TSV) or via in electrical communication with the contact pad, with a claimed centerline that is laterally offset between the first and second elements' pads/vias — the invention description does not mention any TSV structure or an offset-centerline pad/via arrangement, which appears to be a required element the invention lacks
- The core inventive feature emphasized across all claims is the lateral offset between TSV/via centerlines of the two bonded elements (addressing delamination from metal expansion) — the invention's description centers on post-bond anneal-driven copper expansion/fusion without any mention of offsetting via or pad centerlines, suggesting this specific structural limitation may not be present

Note: This patent's claims are directed to a specific structural solution (laterally offset TSV/via centerlines relative to bonded contact pads) for mitigating delamination during hybrid bonding, layered on top of a generic hybrid/direct bonding concept. The invention's copper-to-copper hybrid bonding, CMP planarization, plasma activation, room-temperature bonding, and anneal-driven pad fusion features show potential overlap with the broad hybrid-bonding and direct pad-to-pad bonding limitations common to claims 2, 10, and 15. However, every independent claim requires a TSV or via with a centerline laterally offset from the corresponding centerline in the mating element — a specific structural limitation not described in the invention's feature list. Since claims text does not show any independent claim lacking the offset-centerline/TSV requirement, this is a potentially material distinguishing feature, assuming the invention as described does not include such offset via/pad centerline geometry. This is an informational screening note only, not a legal opinion on infringement or freedom-to-operate. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The note's distinguishing points correctly identify that all independent claims require a TSV/via with laterally offset centerlines, which is a legitimate distinguishing feature since it's an additional required limitation not present in the invention's description — this reasoning is directionally correct (narrower claim due to added limitation means less overlap), not an FTO logic error.
- The statement that claim 10's 'first contact pad at least partially embedded in the first dielectric layer and extending to the first dielectric surface' is 'broad language that could read on the invention's embedded copper pads' is reasonably supported, though it omits that claim 10 also requires the TSV/offset-centerline limitation as part of the same claim, making the isolated quotation slightly misleading about claim scope in context.
- The overlap section's characterization of claims 3-5 and 8-9 dielectric limitations as 'generic enough to potentially cover' the invention's CMP planarization is speculative — the claims say nothing about CMP or planarization specifically, so this is an overstatement beyond what the claim text supports.
- The note appropriately notes claims are pending and may change, which is accurate and not fabricated.

3.32 US20260082960A1 — Bonded structures with integrated passive component

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2026-03-19 · Status: Pending · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claims 1, 3, 11, 13 recite conductive regions of a first surface directly bonded to conductive regions of a second surface without intervening adhesive — this generic hybrid bonding language could encompass the invention's copper-to-copper DBI interconnects as one species of 'conductive regions' bonding.
- Claims 2, 12 recite non-conductive (dielectric) regions directly bonded without adhesive, which broadly reads on the invention's plasma-activated dielectric surface bonding step, without specifying planarization or activation method.
- The general 'hybrid bonded' terminology used throughout (claims 1, 10, 11, 22, 23) is a broad term of art that typically encompasses room-temperature dielectric bonding followed by anneal-induced metal expansion/fusion, which could overlap with the invention's room-temperature bonding and post-bond anneal steps.

Appears to differ (AI reasoning):

- All independent claims (1, 10, 20) require a plurality of capacitors on the backside of the integrated device die forming part of a power delivery network, with specific effective capacitance per unit area thresholds (e.g., at least 200 nF/mm2) — the invention as described contains no capacitor structures or power delivery network capacitance limitations, so this core claimed element appears absent.
- Claims 7, 16, 24 require a high-K dielectric material specifically for the capacitors — the invention's dielectric relates to bonding surface planarization/activation, not a capacitor dielectric, so this limitation appears unmet.

- Claims 5, 6, 15, 21 tie the capacitors functionally to power supply stability for the device die — no such capacitor-based power delivery function is described in the invention.

Note: This patent family centers on bonded structures incorporating integrated passive components (specifically backside capacitors with defined capacitance density) as part of a power delivery network, using hybrid bonding as an enabling/background technique. The invention describes a generic copper-to-copper hybrid bonding (DBI) process itself (planarization, plasma activation, room-temperature bonding, post-bond anneal, alignment), without any capacitor or power-delivery-network element. Overlap exists only at the level of generic hybrid-bonding terminology (conductive/non-conductive region bonding) found in dependent claims 2, 3, 12, 13, which could read broadly on the invention's bonding interfaces. However, every independent claim (1, 10, 20) requires the capacitor/power-delivery-network limitation, which is a structural element not described as present in the invention. Because the capacitor limitation is a required element in each independent claim, the overall relevance is assessed as medium rather than high — the bonding-interface language overlaps, but the capacitor requirement is a significant missing element. This is an informational screening note only, not a legal or infringement conclusion; full claim construction and equivalents analysis would be needed for a definitive FTO assessment. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap statement referencing claims 2 and 12 conflates 'directly bonded without adhesive' non-conductive regions with the invention's specific plasma-activation and CMP planarization steps; the claims are silent on activation method or planarization, so stating this 'broadly reads on' the plasma-activated step is a slight overstatement, though the note does hedge by noting the method is unspecified.
- The claim that 'hybrid bonded' terminology 'typically encompasses room-temperature dielectric bonding followed by anneal-induced metal expansion/fusion' is an assertion about general term-of-art meaning not found in the patent's abstract or claims text provided; this is an inference beyond the given evidence and should be flagged as an unsupported generalization.
- The distinguishing discussion correctly identifies the capacitor/power-delivery-network limitation as a required element in every independent claim, which is a valid distinguishing point (correct direction: absence of an invention feature in dependent claims would be wrong-direction, but here the note correctly emphasizes that the claims require an additional element the invention lacks, which is legitimate distinguishing reasoning, not wrong-direction).

3.33 US20250054854A1 — Heavily doped semiconductor devices for power distribution

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2025-02-13 · Status: Pending · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1 and claim 4 recite two layers with insulating bonding layers 'directly bonded to one another without an intervening adhesive' and (claim 3/4) conductive features 'directly bonded to one another without an intervening adhesive' via hybrid bonding — this generic direct/hybrid bonding language could encompass the invention's copper-to-copper hybrid bonding interconnect (Cu pads embedded in dielectric, bonded without solder).
- Claim 4's requirement that insulating bonding layers be directly bonded together, with conductive features directly bonded on each side, aligns broadly with the invention's dielectric-to-dielectric and Cu-to-Cu bonding scheme (though the claim does not specify planarization, plasma activation, or anneal-driven copper expansion, its broad 'directly bonded' language would still read on an embodiment using those techniques).
- Claim 37's broader bonded-structure claim (insulating bonding layers and conductive features directly bonded without adhesive) is generic enough that it could overlap with the invention's Cu-Cu DBI approach as one possible implementation, subject to equivalents analysis.

- Claim 19/20 bonded-structure claims involving a die conductive feature directly bonded to a device conductive feature without adhesive could overlap with the die-to-wafer bonding step of the invention, again under broad/generic claim language.

Appears to differ (AI reasoning):

- All independent claims (1, 20, 37) require a 'heavily doped semiconductor material' (dopant concentration limits given in claim 12) as a structural layer directly involved in bonding/power distribution; the invention as described does not include a heavily doped semiconductor material layer, so this required element appears absent.
- Claim 1 requires a 'first via extending through the second layer and electrically connecting to the first heavily doped semiconductor material' for power/ground routing; the invention's description does not mention any via structure connecting to a doped semiconductor layer.
- Claim 13/28 require fluid inlet/outlet channels and cooling channels integrated into the insulating layer for liquid cooling; the invention does not describe any fluid cooling channel structure.
- Claim 7 requires dielectric spacers separating heavily doped semiconductor material into islands connected to different potentials — not present in the invention's feature set.
- Claim 37 requires a specific CTE relationship (50%-150% match) between a heavily doped semiconductor material and a device portion of an electronic component — the invention does not specify any doped-semiconductor CTE-matching feature.

Note: The patent's claims center on structures where a heavily doped semiconductor material layer (for power/ground distribution, optionally with cooling channels) is hybrid-bonded to another layer or die without adhesive. The invention's described features (CMP planarization, plasma activation, room-temperature bonding, post-bond anneal, sub-micron alignment) describe a Cu-Cu hybrid bonding *process*, which is not itself recited in these claims — the claims are structural/compositional (heavily doped semiconductor material, vias, cooling channels) rather than process-based. Broad 'directly bonded without adhesive' language in claims 1, 3, 4, 19, 20, and 37 is generic enough to potentially read on an embodiment employing the invention's Cu-Cu DBI bonding scheme, so overlap should be checked at the level of any commercial product embodiment. However, several structural limitations (heavily doped semiconductor material, through-vias to that material, cooling channels, CTE constraints) are central to every independent claim and do not appear to be present in the invention as described, which weighs toward differentiation for those specific claims. This is an informational screening note only, not a legal or infringement conclusion; full claims charting against actual product specifics is recommended. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap statements are accurately grounded in claim text (claims 1, 3, 4, 19, 20, 37 do recite direct/hybrid bonding without adhesive), so these are faithful.
- The distinguishing points correctly note that heavily doped semiconductor material, vias to it, cooling channels, dielectric spacers/islands, and CTE constraints are absent from the invention's feature list and present as required elements in the independent claims — this is legitimate distinguishing reasoning since these are additional required limitations narrowing the claims, not broadening them.
- However, the note's framing that 'the claims do not specify planarization, plasma activation, or anneal-driven copper expansion' being used to support that broad 'directly bonded' language 'would still read on' the invention is fine directionally (absence of process limits makes claim broader/more dangerous), but the note then inconsistently uses the absence of process recitation as part of a paragraph structured as if distinguishing, which could confuse the FTO conclusion — this is a minor internal inconsistency in emphasis rather than a factual fabrication.
- The statement that the invention 'does not include a heavily doped semiconductor material layer' is an assumption based on absence of mention in the feature list; this is reasonable but slightly overstated as a definitive structural conclusion since the invention description may simply not have detailed all layers (minor overstatement, not fabrication).

3.34 US10229897B2 — Multi-layer semiconductor structure and methods for fabricating multi-layer semiconductor structures

Assignee: Massachusetts Institute of Technology · Published: 2019-03-12 · Status: Active · exp. 2035-08-11 · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1 requires planarizing bonding surfaces using CMP prior to deposition of bondable oxide material, which appears to overlap with the invention's dielectric surface planarization via CMP step
- Claim 5 requires precision aligning bonding surfaces to sub-micron accuracy prior to bonding, which appears to overlap with the invention's sub-micron alignment control feature
- Claim 1's initial bonding step (joining active layers/bonding surfaces before the post-bond process) reads broadly on the invention's room-temperature bonding step, though the claim does not specify bonding temperature at this stage
- Claim 1 recites forming vias/interconnects that electrically interconnect bonded structures and create metal layers, which broadly overlaps with the invention's concept of forming continuous metallic interconnects between bonded surfaces
- Claim 8 (dependent) recites performing CMP and annealing on exposed active layer surfaces to prepare for subsequent bonding, which broadly overlaps with the invention's post-bond anneal concept, though directed to a different process stage (surface prep before next bonding, not copper expansion after bonding)

Appears to differ (AI reasoning):

- Claim 1 requires the bonding surfaces to include a specific stacked bondable oxide material (LTO/PSG/BSG combination) as the bonding medium, whereas the invention's bonding is described as copper-to-copper direct metallic bonding without reciting this oxide stack as a requirement
- Claim 1 requires a low-temperature post bond process applied 'at a temperature of at least 150 degrees Celsius', a specific numeric limitation not clearly present in the invention's generic 'controlled post-bond anneal profile' description
- Claim 1's overall method requires a multi-cycle bonding architecture (first bonding cycle, next bonding cycle, filled half-vias, handle removal, 2^n structures/n cycles) that is a specific structural/process framework not described in the invention's simpler two-substrate hybrid bonding flow
- Claim 1 requires 'via last and/or via first' or specific TSV/half-via interconnect formation techniques (per dependent claims 6, 9) which are not described as part of the invention's copper pad expansion/fusion mechanism
- Independent claim 1 does not explicitly recite plasma activation of dielectric surfaces as a step, so the invention's plasma-activation-for-room-temperature-bonding feature is not clearly required by (nor addressed within) this claim's oxide-stack-based bonding chemistry

Note: This patent's independent claim 1 is directed to a multi-cycle wafer-stacking method using oxide-based (LTO/PSG/BSG) dielectric bonding with vias/half-vias for electrical interconnection, rather than a direct copper-to-copper hybrid bonding scheme. Several claim elements (CMP planarization, sub-micron alignment, post-bond thermal treatment, via-based electrical interconnection) are broad enough to potentially read on corresponding invention features, warranting an equivalents-style caution. However, claim 1's specific oxide bonding material stack and specific 150°C+ post-bond temperature limitation, along with the multi-cycle/half-via architecture, are limitations the invention as described does not clearly satisfy. This is an informational screening note, not a legal or infringement conclusion; full claim charting against complete file history and any related claims would be needed for a definitive assessment.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap statement regarding claim 1's initial bonding step reading on 'room-temperature bonding' is overstated: claim 1 requires deposition of a specific LTO/PSG/BSG oxide stack as the bonding medium and a post-bond process at 'at least 150 degrees Celsius,' which is inconsistent with a room-

temperature-bonding characterization; the note's own hedge acknowledges this but still frames it as overlap without adequately noting the oxide-based mechanism differs fundamentally from copper-to-copper DBI.

- The claim 1 overlap on vias/interconnects 'broadly overlaps with the invention's concept of forming continuous metallic interconnects' is weakly supported: claim 1's vias/half-vias are oxide-stack-based interconnect features distinct from the invention's copper pad expansion/fusion mechanism, so characterizing this as overlap with the invention's specific post-anneal copper-fusion feature is an overstatement.
- The distinguishing point stating 'Independent claim 1 does not explicitly recite plasma activation... so the invention's plasma-activation feature is not clearly required by this claim' reasons in the wrong FTO direction: the absence of a limitation in the claim makes the claim broader (and potentially more likely to read on the invention or be silent as to a distinguishing feature), not evidence of non-infringement. A claim not reciting a feature the accused product also lacks reciting is not itself a valid distinguishing factor.

3.35 US20230122531A1 — Reduced parasitic capacitance in bonded structures

Assignee: Adeia Semiconductor Technologies LLC · Published: 2023-04-20 · Status: Pending · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Direct bonding of first and second conductive features (aligned copper features in insulating layers) without intervening adhesive (claims 1, 2, 30) potentially overlaps with the invention's copper-to-copper DBI hybrid bonding without solder microbumps
- Direct bonding of insulating/dielectric layers without adhesive (claims 2, 30) potentially overlaps with the invention's plasma-activated dielectric surface bonding and room-temperature bonding step
- Claim 56's requirement of a direct bonding interface with a surface planarized to low roughness (<2 nm RMS/μm) potentially overlaps with the invention's CMP dielectric planarization step prior to bonding
- General direct hybrid bonding structure/method claims (independent claims 1, 29, 55) broadly recite aligning conductive features prior to bonding, which could read on the invention's sub-micron alignment step in a generic sense

Appears to differ (AI reasoning):

- All independent claims (1, 29, 55) require an 'isolation feature' in the insulating layer between conductive features with a dielectric constant lower than the surrounding insulating layer, specifically for reducing parasitic capacitance — the invention's described features do not include any such low-k isolation feature between bonded pads
- Dependent claims 9-17, 35-36, 40 further specify details of this isolation feature (fill material, width, depth, position, surrounding geometry) that have no counterpart in the invention's disclosed feature set
- The patent's claims do not address post-bond thermal annealing for copper pad expansion/fusion (a central mechanism in the invention); since this is a missing claim limitation rather than a broadening one, it does not itself create overlap, but confirms the patent's claimed focus is on capacitance-reduction structure rather than the copper-fusion bonding mechanism

Note: This patent's independent claims are directed to a bonded structure/method/device where the key limiting feature is a low-dielectric-constant isolation feature between conductive features to reduce parasitic capacitance — an element not present in the invention's described feature set. However, general elements common to hybrid bonding technology (direct Cu-Cu bonding without adhesive, planarized bonding surfaces, aligned conductive features) recited more broadly in claims 1, 2, 29, 30, 55, and 56 show potential overlap with corresponding invention features (DBI copper bonding, CMP planarization, alignment) and warrant closer review of whether an isolation feature equivalent could be read into or is absent from the actual invention implementation. This is an informational screening note,

not a legal or infringement conclusion. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap statement citing claim 56 correctly notes the roughness spec, but claim 56 is dependent on claim 55, which requires the low-k isolation feature; the note's overlap framing does not clearly acknowledge that this claim is still limited by the isolation feature requirement from claim 55, potentially overstating the isolation of the planarization overlap.
- The statement 'General direct hybrid bonding structure/method claims (independent claims 1, 29, 55) broadly recite aligning conductive features prior to bonding, which could read on the invention's sub-micron alignment step in a generic sense' is a stretch: the claims recite conductive features 'aligned' in the final bonded structure, not an alignment process step with sub-micron precision; this overstates the claim scope regarding alignment precision.
- The distinguishing point about the isolation feature being absent from the invention is valid as a distinguishing feature only if the isolation feature is required in all independent claims, which is true here, so this is faithful; however, listing dependent claims 9-17, 35-36, 40 as distinguishing is reasoning in the correct direction since narrower dependent claims add limitations not required by independent claims, so this is fine, but the note should be careful that dependent claims are optional narrowings, not separately assertable as distinguishing from independent-claim risk.
- The note's statement that 'the patent's claims do not address post-bond thermal annealing... since this is a missing claim limitation rather than a broadening one, it does not itself create overlap' correctly identifies wrong-direction reasoning as an issue and appropriately avoids using it as a distinguishing point, which is good practice, but the surrounding language partially reintroduces the missing-limitation-as-distinguishing framing in the final summary paragraph by asking to review 'whether an isolation feature equivalent could be read into or is absent from the actual invention implementation,' which is a reasonable caveat but slightly blurs the FTO direction logic.

3.36 US9716078B2 — Stacked semicondcutor structure and method

Assignee: Taiwan Semiconductor Manufacturing Co TSMC Ltd · Published: 2017-07-25 · Status: Active · exp. 2034-04-10 · Relevance: HIGH · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 1's face-to-face bonded first/second chips with embedded first and second bonding pads in respective dielectric layers, electrically coupled at the interface, broadly reads on the invention's copper-to-copper hybrid bonding interconnect structure between two substrates with embedded copper pads
- Claim 7's requirement that both first and second bonding pads are formed of copper directly overlaps with the invention's copper-to-copper DBI interconnect using embedded copper pads on both bonded surfaces
- Claim 8's 'direct contact' between first and second bonding pads (rather than merely 'electrically coupled') overlaps with the invention's direct metallic copper-to-copper interconnect formed without solder microbumps
- Claim 11's embedding of connection pads and bonding pads within dielectric layers on both chips overlaps with the invention's embedded copper pads within a planarized/bonded dielectric surface
- The general concept of pads on two chips bonded together with post-bonding metallic continuity (claims 1, 8) potentially overlaps with the invention's post-bond anneal step causing pad expansion/fusion, since the claims are broad enough to encompass bonding pads that become continuous/fused after processing, though fusion/anneal is not explicitly recited

Note: This patent (US9716078B2) claims apparatus/structure embodiments of face-to-face bonded chips with embedded copper connection/bonding pads, some in direct contact, which is structurally close to the invention's copper-to-copper hybrid bonding interconnect. Claims 1, 7, 8, and 11 in particular use broad or generic language (e.g., 'copper,' 'direct contact,' 'embedded in dielectric layer') that could encompass the resulting bonded structure of the invention regardless of the specific process (CMP, plasma activation, room-temperature bonding, anneal-induced fusion, sub-micron alignment) used to create it, since these

are method/process limitations not recited in the apparatus claims. This is an informational screening note only, not a legal or infringement conclusion; a full claim-chart and process-vs-apparatus claim analysis by qualified counsel is recommended.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap statement on claims 1, 8 regarding 'post-bonding metallic continuity' potentially overlapping with the invention's post-bond anneal-induced fusion is speculative; the note itself concedes fusion/anneal is not explicitly recited, but framing it as a claim overlap point (rather than omitting it) somewhat overstates support from the claim text.
- The closing note's reasoning that apparatus claims not reciting process limitations (CMP, plasma activation, room-temperature bonding, anneal fusion, sub-micron alignment) means those claims 'could encompass' the invention's structure is correctly used as an overlap-broadening (risk-increasing) observation rather than a distinguishing point, which is the correct FTO direction; however, listing it under a 'Note' after 'Distinguishing points: (none)' could create ambiguity about whether the absence of these features was ever used to distinguish—this should be flagged as a clarity risk though not a logic error, since the note explicitly avoids using it to distinguish.

3.37 US20240096831A1 — Semiconductor package

Assignee: Samsung Electronics Co Ltd · Published: 2024-03-21 · Status: Pending · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claims 1, 14, and 18 broadly claim a semiconductor package with a first chip and second chip each having pads (first pad, second pad) that directly contact one another, surrounded by insulating layers that contact each other — this generic structure of copper pad-to-pad contact with adjoining dielectric layers reads on the invention's copper-to-copper hybrid bonding interconnect with planarized/bonded dielectric surfaces, at least as an equivalent structural configuration.
- The claimed 'first insulating layer...contacting second insulating layer' limitation (claims 1, 14, 18) potentially overlaps with the invention's plasma-activated, CMP-planarized dielectric bonding surfaces, since the claims do not exclude such processing and broadly cover the resulting contacting-insulating-layer structure.
- Claim 11's first/second conductive layers each surrounded by a barrier layer, contacting each other, could overlap with the invention's embedded copper pads that expand/fuse post-anneal, as the claim does not specify how the metallic contact was formed and would encompass a fused copper-to-copper interconnect result.

Appears to differ (AI reasoning):

- All independent claims (1, 14, 18) require the first pad to have an inclined side surface (or first/second side surfaces) forming obtuse angles of about 100° to about 130° with respect to the pad's opposite surface — a specific pad geometry limitation not described in the invention's features, which describe copper pad expansion/fusion after anneal but no specific claimed obtuse-angle sidewall geometry.
- Claim 18 additionally requires a specific stack: an insulating protective layer between the first substrate and first insulating layer, a through-electrode extending through both the substrate and protective layer, and a buffer film spaced apart from the through-electrode — these specific structural elements are not present among the invention's described features.
- Claims 8-9 require specific, distinct insulating materials (e.g., SiO for first insulating layer, SiCN for a lower insulating film of the second insulating layer) — the invention's description does not specify such distinct dielectric materials.
- Claim 13/17 require a first circuit layer below the first substrate, a lower pad, and a first through-electrode connecting the first pad and lower pad — this specific electrical routing structure is not mentioned in the invention's disclosed features.
- Claim 12 requires conductive layers with grooves exposing portions of barrier layers — no such groove feature is described in the invention.

Note: This patent's claims are directed to a specific semiconductor package pad geometry (inclined side surfaces with obtuse angles of ~100°-130°, barrier layers, specific insulating materials, through-electrodes, buffer films), rather than a hybrid-bonding process per se. The invention, as described, focuses on a copper-to-copper hybrid bonding PROCESS (CMP planarization, plasma activation, room-temperature bonding, post-bond anneal, sub-micron alignment) rather than the resulting pad's specific angled sidewall geometry. Broad structural elements in claims 1/14/18 (contacting pads, contacting insulating layers) could potentially overlap with hybrid-bonded structures generally, but the claims' defining and repeated limitation — the obtuse-angle inclined side surfaces — is a specific geometric feature not addressed in the invention's disclosed features, and its presence/absence in the invention's actual bonded pad structure cannot be determined from the given information. This is an informational screening note only, not a legal or infringement conclusion; claims text should be reviewed by qualified patent counsel against full invention drawings/specification, especially pad cross-sectional geometry. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The overlap statements are reasonably grounded, but the distinguishing points repeatedly argue that because the claims do not specify or exclude certain invention features (e.g., 'claims do not exclude such processing', 'claim does not specify how the metallic contact was formed'), this somehow narrows overlap risk — this is backwards FTO logic since claim silence on a feature makes claims broader and more likely to read on the invention, not less risky.
- The note's overlap bullets correctly flag this direction-logic issue in two places by treating claim silence as increasing potential overlap, but the final summary paragraph subtly undercuts this by treating the absence of a discussed feature (obtuse-angle geometry) in the invention description as a clean distinguishing point without acknowledging that the invention's pad after anneal/fusion could still fall within the claimed angle range, which the note admits at the end ('cannot be determined from the given information') — creating some internal inconsistency between the confident distinguishing claim and the later disclaimer.
- Distinguishing claim 8-9 material specifics, claim 12 grooves, claim 13/17 through-electrode/lower pad, and claim 18 buffer film/protective layer limitations are faithfully tied to claim text and invention feature absence, which is appropriate for narrower dependent claims (correct direction), so these are not fabrications.

3.38 US20240186248A1 — Backside power delivery network

Assignee: Adeia Semiconductor Bonding Technologies Inc · Published: 2024-06-06 · Status: Pending · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claims 6, 8, 12, 15, 19, and 26 recite 'hybrid bonded' interconnect elements/dies/power delivery structures in generic terms; this broad language could encompass the invention's copper-to-copper hybrid bonding (DBI) approach as the underlying bonding technology used to join elements.
- Claim 28 recites a method step of 'directly bonding a second element to the bonding surface of the reconstituted element,' which is broad enough to potentially read on the invention's room-temperature direct bonding step prior to anneal, without specifying CMP planarization, plasma activation, or a post-bond anneal profile.
- Claim 29 (integrated voltage regulator directly bonded) similarly uses generic 'directly bonding' language that could read on a Cu-Cu hybrid bonded interconnect if used in that context.

Appears to differ (AI reasoning):

- Independent claims 1, 24, and 28 all require a specific backside power delivery architecture — a via extending from the back side of a semiconductor die to circuitry, a power rail extending from front to back surface of a reconstituted element, and insulating material disposed along the die's side surface — none of which are described among the invention's features (the invention describes a general Cu-Cu hybrid bonding process, not a power delivery network structure).

- Claim 24 additionally requires an insulating material with an embedded power rail and a 'power delivery structure' at the die backside, which the invention's described bonding technology does not include.
- Claims 10, 12, 17, 19 require integrated voltage regulators and/or memory banks in a second reconstituted element — structural/functional elements not present in the invention's feature set.
- Claim 18 requires an optical input/output system bonded to the front surface — not part of the invention as described.
- Claims 21-22 require specific semiconductor die thickness limits (<5 µm or <1 µm) that are not addressed by the invention's disclosed features.

Note: This patent's claims are directed to a backside power delivery network assembly/method (vias, power rails, insulating material arrangement, optional voltage regulators/memory), with hybrid or direct bonding appearing only as one generic joining technique within several dependent claims. The invention as described is focused specifically on the copper-to-copper hybrid bonding process itself (CMP planarization, plasma activation, room-temperature bonding, post-bond anneal, sub-micron alignment) without disclosure of a backside power delivery architecture. Because the independent claims (1, 24, 28) require specific power-delivery structural elements not present in the invention's described features, overlap is likely limited to the generic bonding-step language in select dependent claims. This is an informational screening note only, not a legal or freedom-to-operate opinion. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- Distinguishing points rely on independent claims 1, 24, and 28 lacking the invention's specific bonding features (CMP planarization, plasma activation, post-bond anneal, sub-micron alignment) as a reason overlap is limited — this is wrong-direction FTO reasoning: claims that omit limiting details are broader and thus more likely to read on the invention, not less; the note should flag this as increasing risk rather than as a distinguishing/limiting factor.
- The note's framing that overlap is 'likely limited' because independent claims require power-delivery architecture, while dependent claims 6, 8, 12, 15, 19, 26, 28, 29 use generic 'hybrid bonded' or 'directly bonding' language, is internally inconsistent: those dependent claims are still narrower than the independent claims they depend from (which already recite power rail/via structure), so their broad bonding language doesn't by itself expand scope beyond the independent claim's power-delivery limitations. The note doesn't acknowledge that dependent claims are always at least as narrow as their parent claim, which slightly overstates the potential overlap risk from dependent claims alone.

3.39 US20240063089A1 — Thermal management of base dies in multichip composite devices

Assignee: Intel Corp · Published: 2024-02-22 · Status: Pending · Relevance: MEDIUM · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claims 1, 12, and 18 all recite an integrated circuit die 'hybrid bonded' to a base die, a generic term that encompasses copper-to-copper hybrid bonding/DBI interconnect structures as described in the invention
- The hybrid bonding limitation in these claims is broad enough to read on the invention's use of embedded copper pads forming direct metallic interconnects between dies, without specifying bonding chemistry or process (e.g., CMP planarization, plasma activation, room-temperature bonding, anneal), so the invention's specific hybrid bonding implementation could fall within this broader claim term

Appears to differ (AI reasoning):

- Claims 1, 12, and 18 each require additional structural thermal-management elements (a dummy die with higher thermal conductivity than the inorganic dielectric, a dummy metal via, or microchannels for cooling fluid) that are not described as part of the invention's features; absent such elements, these specific claims would not be met

- Claim 1 and dependents require an inorganic dielectric material laterally adjacent the die and specific dummy die materials/configurations (claims 2,3,7,8,9,11) that are not present in the invention as described
- Claim 12 and dependents require a dummy metal via contacting the base die and structural member (claims 13-17), an element not part of the invention

Note: This patent's independent claims are directed to multichip composite devices with specific thermal-management structures (dummy dies, dummy vias, microchannels) integrated with hybrid-bonded dies, whereas the invention centers on the hybrid bonding process itself (Cu-Cu DBI, CMP planarization, plasma activation, room-temperature bonding, post-bond anneal, sub-micron alignment). The claims' use of the generic term 'hybrid bonded' could broadly encompass the invention's bonding technique as one potential overlap area, but the claims as a whole require additional thermal-management elements not described in the invention, which appear to be missing limitations. This is an informational screening note only, not a legal or infringement opinion; a full claim-by-claim analysis with the specification and prosecution history would be needed for any FTO determination. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The distinguishing points correctly note that the invention lacks the dummy die/dummy via/microchannel elements, but the note frames this as making infringement less likely ('these specific claims would not be met'), while acknowledging elsewhere these are 'missing limitations' from the invention's perspective — this is somewhat contradictory framing; if the invention were incorporated into a device lacking these elements, that would indeed avoid the claims, so this part is actually correctly reasoned (claims require additional elements the invention doesn't have, so narrower claim, less overlap risk — this is correct direction, not reversed).
- The note's FTO direction logic is essentially sound: claims 1,12,18 are independent claims that DO require the dummy die/via/microchannel limitations as affirmative elements, so absence of those elements in the invention is a valid distinguishing point (this is the opposite of the flagged wrong-direction pattern, since here the extra limitation is present in the claim, not absent from it) — no clear wrong-direction reasoning found, so this is a minor stylistic concern rather than a substantive error.
- The claim text for claims 2,7,8,9,11 (dummy die materials/configurations) is correctly cited as dependent limitations not present in the invention, which is faithful to the claim text provided.

3.40 US20250266396A1 — Integrated circuit package and method of forming the same

Assignee: Taiwan Semiconductor Manufacturing Co TSMC Ltd · Published: 2025-08-21 · Status: Pending · Relevance: HIGH · verify on Google Patents ↗

Potential overlap (AI reasoning):

- Claim 16 recites 'forming metal-to-metal bonds and dielectric-to-dielectric bonds between each of the first dies and the first interconnect structure,' which is a broad hybrid bonding limitation that could encompass the invention's copper-to-copper DBI interconnect formed with dielectric bonding, including its planarization and activation steps as generic sub-processes for achieving such bonds
- Claim 1's attachment of die front/back sides to interconnect structures with embedded conductive features (bond pads embedded in dielectric bond layer) is broad enough to read on a copper-pad-in-dielectric hybrid bonding structure like the invention's, without specifying bonding temperature or anneal
- Claim 17's requirement that a die connector contacts a metal pad through dielectric layers, with top surfaces later exposed/leveled, potentially overlaps with the invention's planarized dielectric surfaces prior to copper-to-copper bonding
- Claim 20's step of 'planarizing back sides of the first dies to expose through vias' before forming bond pads is a generic planarization step that could overlap with the invention's CMP planarization step prior to bonding

- The overall method claims' embedding of conductive features/bond pads in dielectric layers with subsequent bonding is broad enough to potentially cover the invention's copper pad embedding and direct bonding structure, subject to claim construction and equivalents

Appears to differ (AI reasoning):

- Claim 19 explicitly requires solder balls and underfill for bonding second dies to first dies, which is a different bonding mechanism than the invention's solder-free copper-to-copper DBI bonding; this claim path does not encompass a solderless approach
- No claim explicitly recites room-temperature bonding or a post-bond anneal causing copper expansion/fusion; claim 16 only generically recites 'metal-to-metal bonds' without specifying a room-temperature step or anneal-driven copper expansion mechanism, so this specific process limitation is not required by the claims as written
- No claim recites sub-micron alignment precision as a limitation; alignment is not addressed in the claims, so this invention feature is not required for overlap analysis (though its absence in claims does not narrow claim scope, it is noted the claims are silent on this specific parameter)

Note: This patent's claims broadly cover multi-tier die/interconnect-structure attachment methods including hybrid (metal-to-metal plus dielectric-to-dielectric) bonding steps (esp. claim 16), which could functionally overlap with the invention's copper-to-copper hybrid bonding process at a generic level. However, the claims as written do not explicitly recite plasma activation, room-temperature bonding, or a post-bond copper-expansion anneal — these specific process parameters from the invention are not claim limitations, meaning claims lacking them cannot be distinguished by their absence (per rules, only claim-required-but-invention-missing elements count as distinguishing). Where claim 19 specifies solder-ball attachment as an alternative bonding method, this represents a genuine claim requirement that differs from the invention's solderless DBI approach for that specific dependent path. Overall relevance is high due to substantial structural and process overlap in multi-die/interconnect hybrid bonding architecture, but this is an informational screening note, not a legal or FTO opinion; full claim charting and prosecution history review would be needed for a definitive assessment. ℹ PENDING APPLICATION (Google Patents): claims may change before grant — monitor for a granted version.

Adversarial auditor annotations (issues the independent audit agent flagged in the note above):

- The note's second distinguishing point states 'this specific process limitation is not required by the claims as written, so it is not required for overlap analysis' — this is correctly flagged by the note itself as not a valid distinguishing basis, but the note still lists it under 'Distinguishing points' framing, which is internally inconsistent and could mislead a reader into treating claim silence as narrowing; this is wrong-direction reasoning even though partially self-corrected in the final paragraph.
- Similarly, the third distinguishing point ('No claim recites sub-micron alignment precision... though its absence in claims does not narrow claim scope') is flagged as a distinguishing point despite the note itself acknowledging this is not valid distinguishing logic — placing it under 'Distinguishing points' is misleading structurally, even though the caveat is included.
- The claim excerpt does not use the term 'copper' anywhere; the note's overlap statements characterizing claim 16's 'metal-to-metal bonds' as potentially encompassing 'copper-to-copper DBI interconnect' is a reasonable inference but slightly overstates specificity, since the claims are generic to 'metal' and 'conductive features' without confirming copper material.

4. Observations (small-sample impressions)

> ⚠ **AI REASONING — MAY BE WRONG.** Impressions from this small sample only — not a landscape analysis.

- Crowded: In this reviewed sample, direct/hybrid copper bonding methods and structures — particularly those involving alignment tolerance, low-temperature bonding, and dielectric/metal surface preparation — appear heavily represented, largely concentrated around filings from Adeia Semiconductor Bonding Technologies Inc.

- Crowded: Room-temperature and low-temperature hybrid bonding process variants (including post-bond anneal type approaches) seem to be a repeated theme across multiple entries in this list, suggesting active prior art density in this specific sub-area.
- Crowded: Stacked device/wafer-level bonding structures generally seem well covered by multiple assignees (Adeia, TSMC, Samsung, Monolithic 3D) in this sample.
- Open: Sub-micron alignment control combined specifically with plasma surface activation as a joint claim element does not appear prominently featured together in this reviewed set, based on titles alone.
- Open: Dielectric surface planarization as a distinct enabling step ahead of copper-to-copper bonding is not clearly emphasized as a standalone focus in most titles reviewed, suggesting possible room for specific process-sequence claims.
- Open: Few entries in this sample explicitly tie post-bond thermal annealing to controlled copper expansion metrics, which may represent a less crowded angle within this reviewed set.
- This summary reflects only impressions from the titles/metadata of the patents listed and should not be treated as a comprehensive freedom-to-operate or novelty assessment.
- Given the high concentration of Adeia Semiconductor Bonding Technologies Inc filings in this sample, a more detailed claim-level review of their hybrid bonding portfolio is recommended before proceeding.
- One entry (US8524533B2) is noted as expired in this list, which may be relevant context but does not by itself open the field given the volume of continuing filings in the same space.

5. Verification Log

Every deep-reviewed patent below was live-fetched from Google Patents structured data at generation time — patent number, title, assignee, dates, claims text and legal status all come from that fetch, not from AI memory, and the engine never estimates dates. Flagged-but-not-reviewed and claims-unavailable entries originate from the real search index (existence shown by the search hit itself); their claims were not analyzed.

Hard-fact ledger: 40 deep-reviewed patents live-fetched & verified at generation time · 89 further hits listed from the search index (existence only, claims not analyzed). Relevance grades, overlap/distinguishing points and observations are AI reasoning over the fetched texts and may be wrong.

Cited fact	Status	Verify
US12532780B2	VERIFIED	open source ↗
US10607937B2	VERIFIED	open source ↗
US20250079364A1	VERIFIED	open source ↗
US20240079376A1	VERIFIED	open source ↗
US20240304593A1	VERIFIED	open source ↗
US20250096191A1	VERIFIED	open source ↗
US12604771B2	VERIFIED	open source ↗
US11911839B2	VERIFIED	open source ↗
US20240088120A1	VERIFIED	open source ↗
US12347820B2	VERIFIED	open source ↗
US12211820B2	VERIFIED	open source ↗

US12354911B2	VERIFIED	open source ↗
US8524533B2	VERIFIED	open source ↗
US12218086B2	VERIFIED	open source ↗
US12616050B2	VERIFIED	open source ↗
US12545010B2	VERIFIED	open source ↗
US20250006674A1	VERIFIED	open source ↗
US11205635B2	VERIFIED	open source ↗
US11742314B2	VERIFIED	open source ↗
US20250006679A1	VERIFIED	open source ↗
US20240332227A1	VERIFIED	open source ↗
US12506114B2	VERIFIED	open source ↗
US20240332231A1	VERIFIED	open source ↗
US20250316625A1	VERIFIED	open source ↗
US12557615B2	VERIFIED	open source ↗
US11121121B2	VERIFIED	open source ↗
US11621249B2	VERIFIED	open source ↗
US12324268B2	VERIFIED	open source ↗
US20250266400A1	VERIFIED	open source ↗
US20240178256A1	VERIFIED	open source ↗
US20250300135A1	VERIFIED	open source ↗
US20260082960A1	VERIFIED	open source ↗
US20250054854A1	VERIFIED	open source ↗
US10229897B2	VERIFIED	open source ↗
US20230122531A1	VERIFIED	open source ↗
US9716078B2	VERIFIED	open source ↗
US20240096831A1	VERIFIED	open source ↗
US20240186248A1	VERIFIED	open source ↗
US20240063089A1	VERIFIED	open source ↗
US20250266396A1	VERIFIED	open source ↗

6. Automated QC & Audit Log

QC battery (qc-battery v1.2): PASSED — 11/11 machine checks.

Check	Result	Detail

features_min3	**PASS**	features=6
search_log_nonempty	**PASS**	queries=6
patents_in_search_set	**PASS**	every reviewed patent ⊆ search set
funnel_accounting	**PASS**	flagged=129 = deep=40 + claims_unavailable=1 + listed=88
stats_consistent	**PASS**	stats.deep=40 vs reviewed=40
deep_means_claims_reviewed	**PASS**	every deep-reviewed patent has actual claims text (no unfetched padding in the deep count)
nonzero_review	**PASS**	zero-review report is not deliverable
direction_rule_scan	**PASS**	wrong-direction distinguishing points in final report=0 required; gate removed 9 upstream
legal_status_coverage	**PASS**	structured legal status on 40/40 fetched patents (≥70% required — below that means the status parser broke)
verification_ran	**PASS**	verification ledger present
disclaimer_present	**PASS**	meta.disclaimer

Adversarial AI audit (claude-sonnet-5): verdict YELLOW — every reviewed patent's analysis was independently re-read against the actual claims text by a separate auditor agent instructed to refute it.

- 40 patent note(s) with minor issues — annotated

7. Legal Notice & Report Status

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